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CHAPTER 1

INTRODUCTION AND DESCRIPTION

PURPOSE OF EQUIPMENT

DECtape Control Type 551 operates up to four Type 555 Dual Tape Transports (eight drives), transferring binary data between tape and the PDP-6 Arithmetic Processor. The Type 551 contains all of the read and write circuitry as well as block detection, error detection, and motion control logic in the DECtape system. Data transfer is accomplished through the Data Control Type 136. A 36-bit data word is assembled or disassembled in the Type 136 for transfer to the DECtape control as 6-bit characters. Individual 36-bit words arrive at the computer approximately every 400 microseconds, and therefore a standard block of 128 words is transferred in 53 milliseconds. The Type 551 is controlled by both the I/O bus and the data control.

FUNCTIONAL DESCRIPTION

The DECtape system stores information at fixed positions on magnetic tape as in magnetic disk or drum storage devices, rather than at unknown or variable positions as is the case in conventional magnetic tape systems. This feature allows replacement of blocks of data on tape in a random fashion without disturbing other prerecorded information. In particular, during the writing of information on tape, the system reads format (mark) and timing information from the tape and uses this information to determine the exact position at which to record the information to be written. Similarly, in reading, the same mark and timing information is used to locate data to be played back from the tape.

DECtape utilizes a 10-track read/write head organized into five channels by connecting pairs of heads in series. The five channels consist of a timing track, a mark track, and three information tracks. Redundant recording of each 5-bit tape character on non-adjacent tracks materially reduces bit drop outs and minimizes the effect of skew. Series connection of track heads within each channel and the use of Manchester phase recording techniques, rather than amplitude sensing techniques, virtually eliminate drop outs.

The timing and mark tracks control the timing of operations within the transport and establish the format of data contained on the information tracks. The timing and mark tracks are recorded prior to all normal data reading and writing on the information tracks. The timing of operations performed by the tape drive and some control functions are determined by the information on the timing track. Therefore, variations in the speed of tape motion do not affect system performance. Information read from the mark track is used during reading and writing data, to indicate the beginning and end of data blocks and to determine the functions performed by the system in each control mode.

During normal data reading, the 551 Control assembles 6-bit bytes from two successive positions read from the information tracks of the tape for transmission to the data control. During normal data writing, the DECtape control disassembles 6-bit bytes from the data control and distributes the bits so they are recorded on two successive positions on the information tracks. Mark track information is recorded serially in six consecutive positions along the tape. A mark track error check circuit assures that one of the permissible marks is read in every six positions on the tape within a block of data.

A tape contains a series of data blocks that can be any length, determined by information on the mark track. Usually a uniform block length is established over the entire length of a reel of tape by a program which writes mark and timing information at specific locations. The ability to write variable-length blocks is useful for certain data formats. For example, small blocks containing index or tag information can be alternated with large blocks of data.

Between the blocks of data are areas called interblock zones. The interblock zones consist of 30 bit- positions before and after a block of data. Each of these 30-position blocks is divided into five 6-position control words. These 6-position control words allow compatibility between DECtapes written on any of Digital's 12-, 18-, or 36-bit computers.

PHYSICAL DESCRIPTION

The DECtape Control Type 551 consists of four Digital standard logic racks and is housed in a Digital standard cabinet. The control may be installed in cabinets with other equipment such as the Data Control Type 136 or the Magnetic Tape Control Type 516; but to avoid confusion assume that a simple cabinet is supplied housing one control and three Type 555 Dual DECtape Transports.

A standard Digital computer cabinet is constructed of a welded steel frame covered with sheet steel. Double doors on the front and rear are held closed by magnetic latches. A full width plenum door provides mounting for power supplies inside the double doors. The plenum door is latched by a spring loaded pin at the top. Module racks are mounted behind the double doors on the front of the cabinet with the wiring side out. Fans mounted at the bottom and top of the cabinet draw cooling air through a dust filter, pass it over the electronic components, and exhaust it through wiring and other openings in the front and top of the cabinet. Four casters allow mobility of the machine and equally share the total system weight of 450 pounds.

Physical Specifications

Dimensions	23-1/2 inches wide, 27-1/16 inches deep, 69-1/8 inches high	
Weight	Logic (4 racks)	30
	Transports (3)	195
	Cabinet	160
	728 Power Supply	20
	778 Power Supply	25
	811C Power Control	18
	828 Power Control	2
		450 pounds
Service Clearances	8-3/4 inches in front, 14-3/4 inches in back	
Color	Blue	
Operating Temperature	50 to 105°F ambient	
Thermal Dissipation	2150 Btu/hour	

ELECTRICAL DESCRIPTION

DECtape Control Type 551 requires 6.5 amperes (8 amperes surge) at 115 volts, 60 cps. Power connection is through a Hubbell Twistlock plug rated at 30 amperes and 250 volts ac. All signal cables plug into 22-pin connectors mounted in the logic racks. The required cables are four I/O bus cables, two data control cables, one Type 555 to 551 head cable, and one Type

555 to 551 selection cable. Each additional Type 555 Transport (after the first) requires a head jumper cable and a selection jumper cable (lengths dependent upon system configuration).

PERTINENT DOCUMENTS

The following documents serve as source material and complement the information in this manual:

a. Programmed Data Processor-6 Handbook, F-65. This handbook provides complete programming instructions for the DECtape system.

b. Programmed Data Processor-6 Maintenance Manual, F-67. This manual contains general maintenance instructions for the Type 166 Arithmetic Processor and its interface with peripheral I/O equipment.

c. Programmed Data Processor-6 Circuit Manual, F-67 (166 Cir.). This manual gives maintenance instructions for the basic circuit elements and modules comprising the DECtape system.

d. System Modules Catalog, C-100. This catalog presents information pertaining to the function and specifications of the basic systems modules and module accessories comprising the DECtape control.

e. DECtape Dual Transport Type 555 Maintenance Manual, H-555. This manual provides maintenance information for the transport portion of the DECtape system.

f. Data Control Type 136 Instruction Manual, H-136. This manual presents maintenance information for the data control portion of the DECtape system.

Additional copies of all items are obtained from the nearest Digital district office or from:

Customer Relations Department
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

CHAPTER 2

SYSTEM DESCRIPTION

A PDP-6 DECtape system consists of three peripheral elements: the Type 136 Data Control, the Type 551 DECtape Control, and up to four Type 555 Dual DECtape Transports. Figure 2-1 shows the relationship between the components of the system. The Type 166 Arithmetic Processor communicates to both the data control and the DECtape control via the I/O bus. Data flows in 3-bit bytes between the DECtape transports and the DECtape control, in 6-bit bytes between the DECtape control and the data control, and in 36-bit words between the data control and the arithmetic processor. The data control and the DECtape control are independent devices; but when both are given commands to perform an operation, they synchronize with each other without further aid from the arithmetic processor. The arithmetic processor must respond to flags raised by the data control when the transfer of a 36-bit word is required.

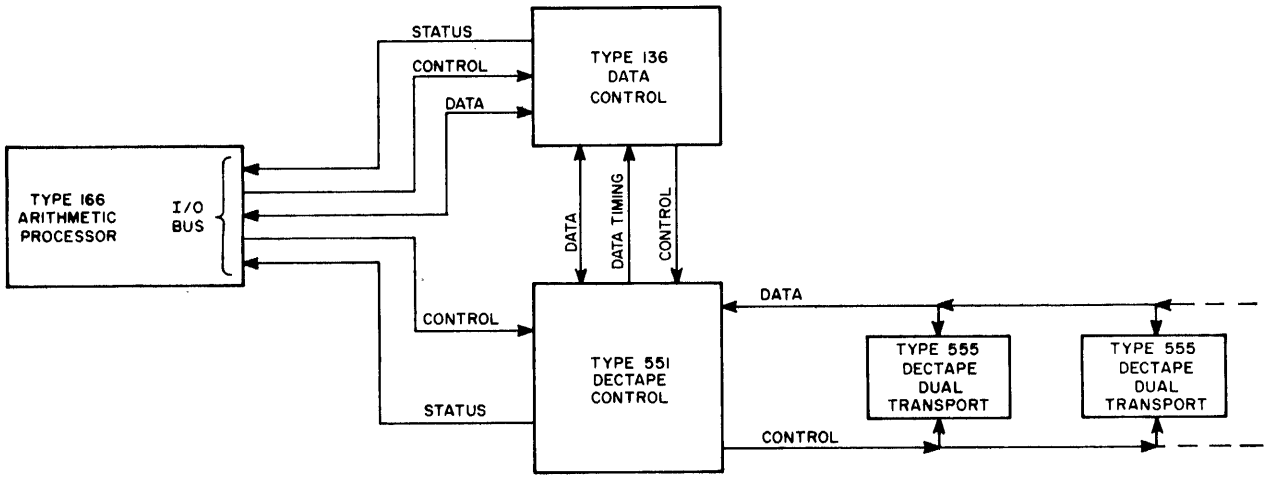


Figure 2-1 DECtape System Block Diagram

DATA CONTROL TYPE 136

The data control contains two 36-bit registers: a data accumulator for communicating with in-out devices, and a data buffer for communicating with the arithmetic processor. The direction of data flow depends on commands given by the arithmetic processor. During input operations,

data from the selected device accumulates in the data accumulator until 36 bits of information are present. Then the contents of the data accumulator are transferred to the data buffer, a flag is raised, and the data accumulator becomes ready to accumulate more data. The arithmetic processor can respond to the raised flag and process the information while the data accumulator is refilled.

For output operations the flow is reversed. The arithmetic processor places data in the data buffer. When the data accumulator is empty, the data control refills the data accumulator from the data buffer and raises a flag signaling that the data buffer is free. While the DECtape control (or other device) is taking data out of the data accumulator, the program must compute the next data and refill the data buffer. For both input and output, the arithmetic processor is given the longest possible time to perform its functions.

DECTAPE CONTROL TYPE 551

DECtape Control Type 551 controls the motion and read-write operations of up to four Type 555 Dual DECtape Transports (eight drives). Because DECtape records three bits at time, the Type 551 converts the 6-bit bytes which are transmitted between the data control and itself into two 3-bit bytes. The DECtape control reads and checks the timing and control information which must be prerecorded on each DECtape reel. Tapes are written or read while moving in either direction. The DECtape control also contains the facilities for prerecording timing and control information.

DECTAPE TRANSPORT TYPE 555

The Dual DECtape Transport Type 555 consists of two electrically identical transports and the associated motors and control logic. All read/write electronics are contained in the DECtape control. Switching logic in the Type 555 controls motor action and read/write head selection.

RECORDING FORMAT

DECtape utilizes a 5-channel format. On tape, each channel is recorded in two non-adjacent tracks. A channel consists of electronics and two read/write heads in series. Redundant recording of each channel on non-adjacent tracks materially reduces bit drop outs and minimizes

the effect of skew. Three channels are assigned for the recording of data, one channel for timing information, and one channel (called the mark track) for control and format information. Track placement is shown in Figure 2-2.

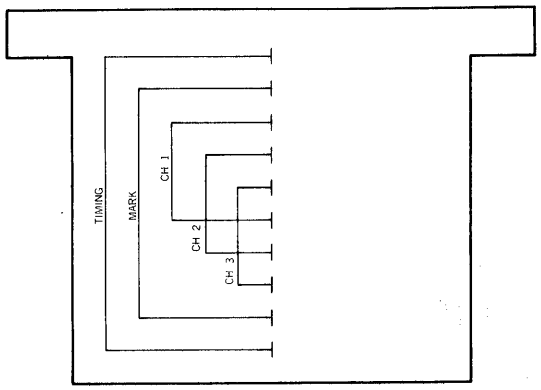


Figure 2-2 Placement of DECtape Tracks

Manchester Recording

Data is recorded by the Manchester method in which a prerecorded timing track synchronizes read-write operations. When writing on the tape, the write amplifiers always supply the maximum current in one direction or the other (non-return to zero, NRZ). To write a pulse, the polarity of the write current is reversed. The polarity of the pulse thus produced depends on whether the write current underwent a positive or negative transition. The timing track is prerecorded with alternate positive and negative transitions at fixed time intervals. The negative transition is used only during writing and is a signal to load the write buffer. The positive transition is used during both reading and writing. During writing, this transition is a signal to switch the polarity of the write current in all write heads. If a zero is being written, the current, which starts out positive for writing zeros, is switched to negative thus creating a negative transition. If a one is being written, the current starts out negative and generates a positive transition when switched to positive. During reading, the positive transition of the timing track is a signal to strobe the data and mark track read-amplifier outputs into the read buffer. If a positive transition is sensed at strobe time, a one is placed in the buffer; otherwise a zero is strobed in.

The Manchester system has several advantages. Because the strobe is a relatively narrow pulse, the system is immune to noise outside the strobe time. At strobe time, all data signals are

negative pulses representing zeros or positive pulses representing ones. These pulses are all at their peaks. Thus, to have any effect, a noise pulse must be great enough to reverse the polarity of a data pulse. Few noise pulses are that large. Another advantage is that data can be written immediately adjacent to previously written data because timing is rigidly controlled from a timing track written on the tape.

Redundant Recording

The recording of each channel on two non-adjacent tracks has several advantages. A speck of dust or a flaw in the tape must extend over both tracks of one channel to cause misreading. Noise must be of sufficient amplitude to exceed the sum of the signals from both tracks in order to have any effect. The signal from either track alone is sufficient for proper reading. The timing tracks are the two outermost and thus are subject to the greatest skew. Pulses from other tracks occur between the summed pulses from the timing tracks; therefore, the effects of skew are averaged out.

MARK TRACK FORMAT

One of the five DECtape channels is reserved for control information exclusively. Control codes are stored serially, six bits per code. These codes control such functions as marking the beginning and end of data, the checksum, the block number, the end of tape zone, and others. These codes are automatically identified by the DECtape control which controls the transmission of data accordingly.

Because the DECtape system allows reading and writing in both directions of tape motion, the mark track is often read in reverse. In that case, not only are the mark track bits read serially in the reverse order; but also, since the polarity of pulses is reversed when the tape moves backwards, the complement is read. The complement of a number with the bits reversed is defined as the complement obverse. The mark track format has been carefully selected to be symmetrical so that the logic for reading in the reverse direction is exactly the same as that for the forward direction. The complement obverse of the end of tape mark becomes the beginning of tape mark, and the end of data mark becomes the beginning of data mark, for example.

Bits that are read from the mark track are shifted into a shift register to identify the mark. The mark codes are chosen so that (with one exception, block-mark space described below) the intermediate stages of shifting cannot result in a valid mark code. The DECtape can be stopped and started at any point without the possibility of confusing the DECtape control. The DECtape control readily synchronizes with the mark track from any starting point.

BLOCK FORMAT

The block format is essential to the operation of DECtape. The entire usable length of tape is divided into fixed length blocks as determined by information recorded in the mark track. Although block length is arbitrarily determined when the mark and timing tracks are recorded, 128-word blocks are considered standard on the PDP-6. Blocks are symmetrical so they can be written or read with equal facility in either direction.

Each block consists of the information shown in Figure 2-3. Between each block of data, a number of control words appear, collectively called the interblock zone. Words in this zone are used for block identification, error checking, and control purposes.

Because three bits are written on the tape at one time, 12 bit times are required to write a full 36-bit word. During the 12 bit times, two mark codes appear since each requires 6 bit times. When 18 bits of data are sufficient for fulfilling format requirements in the interblock zone, only one mark code is reserved.

Block Mark, Block-Mark Space, Block-Mark End

A block begins and ends with a number of words used for timing and control functions. The first of these is the block mark which is a 36-bit number used as a label in programming to locate a desired block of information. A tape prerecorded in the standard manner has block marks numbered from 1 to 1100_8. Two mark codes appear in the mark track opposite the block mark. These are block-mark space (25_8) and block-mark end (26_8). The reading or writing of a block mark actually begins in the preceding block (see Block-Mark Sync below). For this reason, the first and last block marks on a reel of tape cannot be read. Therefore, dummy blocks with block marks 0 and 1101_8 are provided.

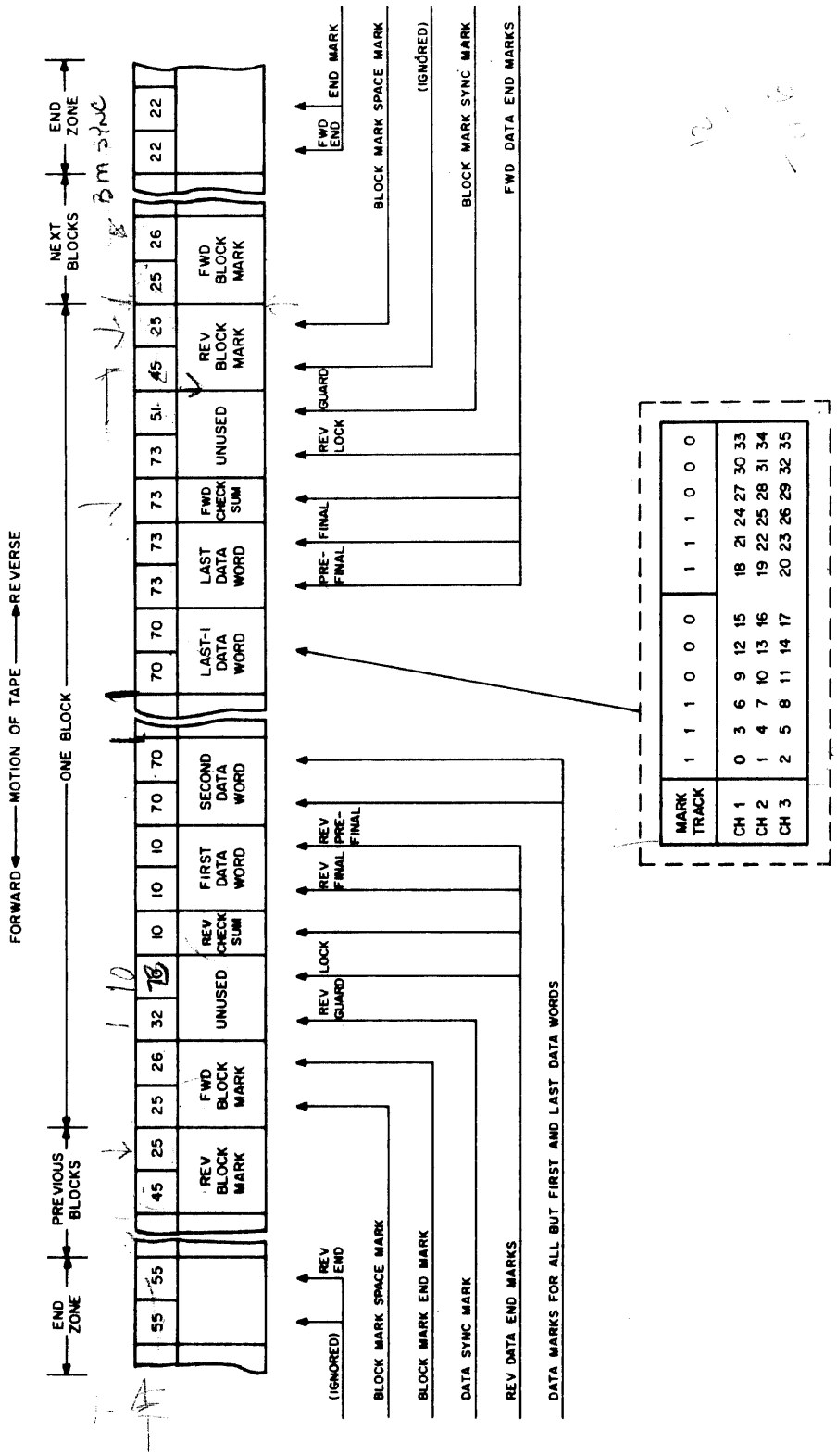


Figure 2-3 Mark and Information Track Formats

The block-mark end signals the completion of a block mark. The block-mark space, in the position described here, has no function in the forward direction. However, this mark is its own complement obverse and therefore appears again opposite the reverse block mark at the end of the block, immediately adjacent to the block-mark space which is part of the following block. This mark consisting of alternate ones and zeros in its binary representation is the only mark which legitimately occurs more often than once in six bit positions. (See below, Block Mark Timing Register, for an explanation of how block marks are read.)

Data Sync

Data sync is a mark track code (32_8) signifying that data follows. It is used to synchronize data transmission operations so that transmission begins following the next checksum. If, due to a mark track error, data transmission is in progress while this mark is read, transmission is stopped, and an error flag is raised. The 18 bits of data opposite the data-sync mark are unused.

Reverse Data-End Mark

Reverse data end is a mark-track code (10_8) which appears four times in succession. The four appearances have the following meanings.

First Appearance

The 18 bits of data opposite the first appearance of reverse data end comprise the lock mark. This slot is present for timing purposes; it provides additional time in which the arithmetic processor can command the DECtape control to switch from reading block marks to reading or writing data.

Reverse Checksum

The 18 bits of data opposite the second appearance of reverse data end comprise the reverse checksum. For symmetry purposes, there is a checksum at each end of a data block. The checksum is a parity check (the exclusive OR, not the arithmetic sum) of all 6-bit bytes transmitted between the data control and the DECtape control. The six bits of the checksum are written out once, and the remaining 12 bits of the checksum slot are filled out with ones. If a data

block is written in the forward direction, the reverse checksum is preset to 007777_8. If, however, the data block is written in the reverse direction, the reverse checksum contains the computed checksum. The parity computed is the parity of zeros. The checksum is preset so that the final result, if correct, is all ones. During reading, the checksum of all words, including both the reverse and forward checksums, is recomputed automatically; and if the result is not all ones, the parity error flag is raised.

First Data Word

The third and fourth appearances of the reverse data end delimit the first 36-bit data word.

Data Mark

The data mark is a mark-track code (70_8) which delimits all 36-bit data words from the second to the next-to-last word in a block. Every two data marks delimit one 36-bit word. A 2-word block requires no data marks because the reverse final, reverse prefinal, prefinal, and final marks are sufficient to delimit two data words. A 0- or 1-word block is improper and cannot be read. Longer blocks have as many data marks as required to delimit all data words. The data mark is its own complement obverse so that the same mark delimits data words in both directions of tape motion.

Forward Data End Mark

The forward data end mark is the complement obverse of the reverse data-end mark. The functions of forward data end are symmetrical to the functions of reverse data end which is discussed above.

Block-Mark Sync

Block-mark sync is the complement obverse of data sync. When read in the forward direction, block-mark sync prepares the DECtape control for reading the block mark in the next block. If, due to a mark-track error, data transmission is in progress when this mark is read, transmission is stopped and an error flag is raised thereby protecting the block marks that follow.

As with the data sync mark, the 18 bits of data that accompany the block-mark sync are unused.

Reverse Block Mark

The reverse block mark completes the symmetry of a standard block. The two mark-track codes that delimit the reverse block mark are 45_8 (the complement obverse of block-mark end) which is ignored and 25_8 (block-mark space) which is its own complement obverse and is discussed above. The forward block mark of the next block immediately follows the reverse block mark.

Reverse and Forward End Marks

The first and last few feet of each reel of DECtape are devoted to consecutive end-mark codes. The forward end marks (22_8) appear at the end of the tape, and when read in the forward direction, cause the DECtape control to stop tape motion. The reverse end mark (55_8, the complement obverse of the forward end mark) is ignored. Therefore, a tape which has moved into the end zone can be moved back into the center of the tape with no difficulty but under program control can be pulled off the reel only with the greatest of difficulty.

REGISTERS OF THE TYPE 551

In order to understand the operation of the Type 551 DECtape control, it is helpful to be familiar with the hardware registers involved. Although some of the registers cannot communicate directly with the program, knowledge of the functions they perform makes understanding the operation of the overall system somewhat simpler. Figure 2-4 is a block diagram showing the relationships of the registers of the Type 551.

Control Register

DECtape Control Type 551 uses more than 18 bits of control and status information. Therefore, two device numbers are assigned, 210 and 214. Device 210 refers to the control register. Commands to the DECtape control are encoded in the bits sent to this register which have the following meanings:

Bits	Meaning
19	if 1, select tape unit; if 0, deselect all tape units
20	tape-end enable - if 1, permit tape end mark to cause an interrupt
21	job-done enable - if 1, permit job-done flag to cause an interrupt

To be supplied

Figure 2-4 DECtape Control Type 551 Block Diagram

Bits	Meaning
22	go - tape moves if 1, tape stops if 0
23	reverse motion if 1, forward motion if 0
24	time enable - if 1, permit time flag to cause an interrupt
25, 26	start-stop delay encoded as follows: 00 = no delay 01 = reselection delay, tape is moving but another unit was selected (35 msec) 10 = turn-around delay (225 msec) 11 = start delay (300 msec)
27, 28, 29	command function encoded as follows: 0 = no data transmission 1 = read all tape as a single record, beginning with the next reverse block mark 2 = read the next block number 3 = read data until the data control disconnects 4 = write timing and mark track (the WRTM enable switch must be on or this command will not be executed) 5 = write all tape as a single record beginning with the next reverse block mark 6 = write the next block number 7 = write data until the data control disconnects (the last block is filled out with whatever happens to be in the data accumulator and the checksum is written automatically)
30, 31, 32	tape transport number - 0 is transport 8, 1 through 7 are transports 1 through 7
33, 34, 35	interrupt channel number

For a complete description of each of the functions above, see Chapter 5, Operation.

Status Register

The status register contains all flags that reflect the condition of the DECtape control. Bits 29 through 35 are cleared when any CONO command is given to the command register (device 210). The status register is device number 214. The bits have the following significance:

Bits	Meaning
25	start delay - set to 1 during a delay
26	read-write request state - data transmission has been momentarily suspended but will resume when the tape is in position
27	read-write active state - data transmission is occurring
28	read-write null state - either a delay is in progress or data transmission has ceased and will resume only when further commands are received
29	incomplete block flag - set to 1 if the data control disconnects in the middle of a data block
30	write enable - a synchronizing level set to 1 upon entering the active state, and set to 0 upon leaving the active state
31	time flag - set to 1 on completion of the specified time delay
32	information error - set to 1 if a checksum or active mark-track error occurs
33	illegal operation - set to 1 when attempting to write when the write lock switch is on, attempting to write the mark track when the WRTM switch is off, not attempting to write the mark track when the WRTM switch is on, or attempting any operation if more than one or if no unit is selected
34	tape-end flag - set to 1 when the selected tape moves into the end zone; tape motion is stopped when this flag is set
35	job-done flag - set to 1 after completion of reading or writing data when the last checksum has been processed or immediately after reading or writing block marks

Read-Write Buffer

The read-write buffer (RWB) is a 6-bit register which transmits data between the data control and the read-write heads. This buffer communicates with the high order end of the data accumulator during forward operations and with the low order end during reverse operations.

Longitudinal Buffer

The longitudinal buffer (LB) is a 6-bit register in which the checksum is computed. During reading and writing, the complement of each 6-bit byte that enters the read-write buffer is exclusive-ORed into the longitudinal buffer. At the end of a block, the contents are written out as the checksum when writing; or the checksum read from the tape is exclusive-ORed into the computed checksum and the result compared with one when reading.

Mark Track Window

The mark track window (TMK) is a 9-bit shift register into which are shifted bits read from the mark track. Because the mark track window is three bits longer than required to contain one mark, additional redundance is thereby provided to check that marks follow one another in the proper order. The bits of the mark track window are continuously decoded to detect when any of the legal marks have appeared.

Error Check Register

The error check register (μTEK) is a 6-bit shift register which checks that a legal mark-track mark occurs exactly every six bit times. The block-mark sync (25_8) is the only mark which legitimately occurs in other than six bit positions from the previous mark; therefore, this mark presents the error check register to 100000_2. This register is shifted every bit time. When the 1 reaches the low end of the register, a check is made that a legitimate mark is present. At all other bit positions, a check is made that no legitimate mark is present. The failure of either check raises the information error flag and stops data transmission.

Block Mark Timing Register

The block mark timing register (TBM) is a 4-bit shift register which controls the timing of reading and writing block marks. A 1 is shifted into TBM0 when the block-mark sync is read from the mark track. This 1 is shifted through the block-mark timing register each time the block-mark space appears in the mark-track window. As previously noted, the block-mark space consists of alternating ones and zeros, and being preceded and followed by alternating ones and zeros, is detected in the mark-track window every two bit times instead of the normal six. Therefore, on the third shift the 1 shifts into TBM3, just as the forward block mark is moving into position to be read or written.

Data Timing Register

The data timing register (TDATA) is an 8-bit shift register which controls the timing of reading and writing data and writing or checking the checksum. A 1 is shifted into TDATA0 when the data sync mark is read from the mark track. The register is shifted whenever data sync, forward data end, or reverse data end is read from the mark track for a total of nine shifts per block. The DECtape control initializes the checksum when the 1 shifts into TDATA1, and writes out or checks the checksum when the 1 shifts into TDATA6. This register also controls stopping data transmission during interblock zones.

CHAPTER 3

THEORY OF OPERATION

Throughout the following chapter, reference is made to the drawings reproduced in Appendix 1. A set of full-sized drawings is supplied with the equipment; and where a discrepancy exists between the drawings in this manual and the full-sized drawings, assume that the latter are correct. Drawings are referred to by the letters at the end of the full drawing number. For example, drawing RWB is drawing BS-D-551-0-RWB.

BLOCK SCHEMATIC DISCUSSION

Initialization Operations

All operations of the DECtape control begin with a CONO command to device 210. In addition to the operations involved in filling the command register, certain other operations, such as the initial time delay, are common to all DECtape functions.

I/O Bus Interface

The I/O bus interface with the Type 551 DECtape Control is shown on drawings UTC1 and UTC2. Command pulses and levels enter drawing UTC2 at the left. The device number to which the command on the I/O bus is addressed is sent as seven pairs of complementary signals. The appropriate member of each pair is applied to two NAND gates at 1D17 to decode the two DECtape device numbers 210 and 214.

During a CONO command, two pulses are issued on the I/O bus. The first, IOB CONO CLEAR, triggers the UT CONO CLEAR pulse (see the upper left of drawing UTC2) to clear both the command and status registers when the command register is addressed. The IOB RESET pulse also triggers UT CONO CLEAR so that pressing the I/O RESET key on the Type 166 Arithmetic Processor console stops the current operation of the DECtape control.

The second pulse on the I/O bus is IOB CONO SET, which commands the addressed device to read the data lines into its control register. This pulse, ANDed UT SELECT (210), initiates

both the UT CONO SET pulse (0.4-microsecond width) and the UT CONO SET LONG pulse (1.0-microsecond width). All circuits which receive UT CONO SET LONG trigger on the trailing edge, thereby achieving a 1-microsecond delay after UT CONO SET.

The command register consists of the Type 4217 Flip-Flop modules shown on drawing UTC1. The UT CONO CLEAR pulse clears the entire register simultaneously, and the UT CONO SET pulse reads the I/O bus data lines into the register.

Initial Time Delay

The initial time delay circuits are shown at the bottom of drawing UTC1. The outputs of the two flip-flops that store the delay-specification bits, UT TIME0 and UT TIME1, are applied to a NOR gate at 1B5 to produce the UT TIME level whenever a nonzero delay time is required.

The outputs of UT TIME0 and 1 also enable one of the three delay control units at 1B3. UT START is a controlled delay, triggered by the trailing edge of UT CONO SET LONG. The output of UT START remains in the 1 state from UT CONO SET LONG time to the end of the requested delay period. The transitions of the UT START delay provide delayed pulses required in portions of the circuits discussed later.

Tape Unit Selection

Four flip-flops of the command register control which DECtape drive is selected. The outputs of these four flip-flops, UT UNITS SELECT and UT UNITS 0 through 2, are applied to a 4-bit binary-to-BCD decoder. Only the 0 through 7 decoder outputs are used. The extra flip-flop, UT UNITS SELECT, makes possible the deselection of all units. Because the BCD decoder interprets correctly only 10 of the possible 16 input combinations, having UT UNITS SELECT contain 0 is not sufficient to deselect all units; UT UNITS 0 and 1 must also contain 0. Ground is applied to the one line in eight corresponding to the selected unit (or, if no unit is selected, all lines are at -3 volts). The DECtape transport that is dialed to the grounded line responds to the transport control signals and connects its read-write heads to the head signal lines.

The normal ground input to pin D of the Type 4671 is disconnected and a 2-ohm resistor to ground is inserted instead. This resistor develops an analog signal, UT UNIT CHECK, that is measured

to determine how many units are responding to the unit-selection signal. This signal is compared in differential amplifiers at 1B8 (drawing UTE, the right-hand side) with preset bias voltages to form the UTE UNIT OK level when exactly one unit responds to the unit selection signal.

Tape Motion Selection

Two flip-flops of the control register, UT GO and UT REV, determine the motion of the selected unit. The UT GO flip-flop drives solenoid drivers which, in turn, drive relays in the selected unit to start or stop tape motion. Similarly, the UT REV flip-flop selects forward or reverse motion.

Two logical conditions, in addition to a direct CONO command from the arithmetic processor, can set the UT GO flip-flop to 0 and therefore stop the motion of the selected tape. The conditions are: more or fewer than one transport selected (not UTE UNIT OK); and tapemoving into the end zone (UT TAPE END FLAG (1), see mark track decoding). Note that UTE UNIT OK is tested only at the end of the initial delay time (the leading edge of UT START (0)); if no delay is selected, this check is inoperative.

Command Decoding

The DECtape command is encoded in the three bits stored in flip-flops UT FCN0, UT FCN1, and UT FCN2. The command encoding is chosen so that all write operations have a 1 in UT FCN0. Therefore, the UT FCN0 (1) level is buffered (see the upper left of drawing UTC1) and renamed UT WRITE; the complement of UT WRITE is UT READ. These levels are used throughout the DECtape control to distinguish between read and write operations.

Because read and write operations are distinguished by special signals, it is unnecessary to decode such pairs as read data and write data as separate commands. Therefore, several of the outputs of the Binary-to-Octal Decoder Type 4151 that decodes the command function are connected together. For example, the read data and write data commands are decoded as a single level, UT DATA. Similarly, the UT BM (read or write block marks), and the UT ALL (read or write all) levels are developed. The two remaining commands are not combined. These are the do nothing command which produces the UT DN level and the write timing and mark track command which produces the UT WRTM level.

Operations Common to All DECtape Functions

The following operations are common to all DECtape control functions. The only requirement for these operations to occur is that a transport is selected and in motion.

Timing Track Reading And Time Pulse Generation

The timing track read-write head cable enters the DECtape control at 1A22 (as do all read-write head cables). The center-tap wire is grounded and the two signal wires enter the read amplifier through a maintenance jumper-plug at 1A55 (see drawing TMT). The read amplifier is a high-gain amplifier having a pair of complementary, standard logic level outputs. The outputs are applied to pulse generators to produce the principal timing pulses, TT1 and TT0. TT1 is the read strobe pulse and TT0 is the write complement pulse.

The time-pulse chain appears in drawing TMT at the upper right. The chain consists of a series of pulse amplifiers, each triggered by the positive overshoot of the trailing edge of the output from the previous stage. Time pulse generation is inhibited during the 8 microseconds following each TP0 and (during write operations) following each TP1 by the T CROSS TALK delay. The delay prevents stray pulses and cross-talk from interferring with normal operation. The timing track pulses are also inhibited while writing the mark and timing tracks because, at that time, the time-pulse chain is triggered by the output of a clock.

Mark Track Decoding

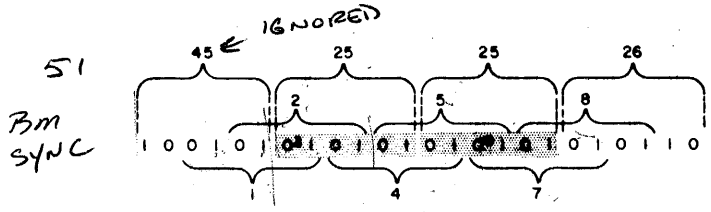
Mark track decoding is performed by a Type 4260 Mark Track Decoder, a special-purpose module. The output of the mark-track read amplifier (similar to the timing-track read amplifier) is shifted into TMK0 every TP1 (read strobe) time except while an initial delay is in progress or when the mark track is being written. The TMK register is set to 0 at the start of the initial delay by the T CLEAR pulse. Bits shifted into TMK0 progress through the register up through TMK7. Only ones are shifted from TMK7 to TMK8; a 1 in TMK8 indicates that at least nine shifts have taken place since the last time TMK was cleared; a 1 in TMK8 is required in decoding all marks. The outputs of the TMK register are applied to eight AND gates to recognize specific mark track codes. To be detected, a mark track code must not only agree in its six positions, but the last two positions of the preceding code must also agree and at least nine shifts must have occurred since the last clearing of TMK.

If the tape moves into the end zone while data transmission is occurring, the UT TAPE END FLAG(1) level, applied to the capacitor-diode gate at the lower right of drawing RWBC, sets up the RW NULL state, thus stopping data transmission.

Write Block Mark Operation

Block Mark Timing Register Operation

The block mark timing register (TBM) is a 4-bit shift register appearing in drawing TMT. At TP2 time, this register is shifted one place if either block mark sync (MK BM SYNC) or block mark space (MK BM SPACE) appears in the mark track window. A 1, shifted into TBM0 when block mark sync is read, is shifted three times while block mark space is read. The figure below, showing the binary representation of the mark track codes involved, illustrates how block mark space appears in the mark track window every two bit times.



Block mark space continues to appear in the mark track window every two bit times for a total of eight appearances, thus shifting the 1 completely out of the block mark timing register. Most of the important functions occur when the 1 shifts into TBM3 signifying that the block mark is about to come under the read-write heads.

Data Transmission Control

The data transmission control circuits are shown in drawing RWBC. The circuit shown at the lower right of drawing RWBC is of greatest importance. The three positive NOR gates at 1B5 form a tristable circuit similar in many ways to an ordinary bistable flip-flop. The one NOR gate whose output is ground enables the other two gates so that their outputs are -3 volts.

The three outputs are three very important logic levels, RW NULL, RW RQ, and RW ACTIVE. The UT CONO CLEAR pulse, applied to a capacitor diode gate at 1D2 places the circuit in the RW NULL state upon receiving each new command. In this state, all data transmission is inhibited.

The next circuit action depends on whether an initial time delay is selected. If no delay is selected, the UT CONO SET LONG pulse, applied to a capacitor-diode gate enabled by NOT UT TIME, sets up the RW RQ state. Otherwise, the transition of UT START going to 0 at the end of the delay period sets up the RW RQ state. In the RW RQ state, the DECtape control waits for the proper marks to be read from the mark track before transmitting data. In the case of write block marks, the control waits for a 1 to shift into TBM3.

At TP2 time just before the first bits of the block mark must be written out, a 1 shifts into TMB3. The resulting transition, applied to a capacitor-diode gate at 1B7 sets up the RW ACTIVE state.

Once in the active state, a host of actions is enabled. The first action occurs in drawing TMT. The TCT flip-flop controls the separation of each 6-bit character from the data control into two 3-bit bytes. The capacitor-diode gate AND circuits at the complement input to this flip-flop ensure that it returns to the 0 state when data transmission is not active. The RW ACTIVE level begins too late to complement TCT on the same TP2 that shifted the 1 into TBM3 because of the delay of the capacitor-diode gates.

A NAND gate in the lower left of drawing RWBC produces the RW ODD signal when RW ACTIVE and TCT(0) are both present. RW ODD enables a capacitor-diode gate which triggers the RW CLEAR pulse at TP3 in preparation for accepting the block mark data.

RW ODD also enables the logic at the upper right of drawing RWBC to produce a RWB ⟷ DC pulse on the next TP4. The TDATA register is cleared (see Data Write Operations) and the command is not UT WRTM; therefore, a pulse is produced each TP4. At this point in the logic, the direction of tape motion makes a difference. If the direction is reverse, the complement obverse of the data must be formed so that reading back in the forward direction requires no data manipulation. The obverse is formed by commanding the data control to shift right instead of left and by accepting bytes from the right end of the data accumulator instead of the left end. The complement is formed in the write buffer logic as explained below. Therefore, the RWB ⟷ DC pulse triggers either (LT) RWB ⟷ DC(1) FWD or (RT) RWB ⟷ DC(1) REV depending on whether the tape motion is forward or reverse respectively.

The read write buffer (RWB) appears in drawing RWB. One of two sets of capacitor-diode gates reads the 6-bit byte from the appropriate end of the data accumulator into RWB. Simultaneously, the data control starts to shift the next 6-bit byte into position. Information from the left end of the data accumulator enters via a plug at 1D25; the right end enters via 1D24.

The sequence of clearing RWB on TP3 and refilling it on TP4 whenever TCT contains 0 continues until the 36-bit block mark is written. Since TCT complements on every TP2, a new 6-bit byte is requested every two bit times.

Data Write Control

At the next TP0, the data must enter the write amplifiers and writing must commence. If tape motion is in reverse, the complement of RWB must be written (the obverse is formed previously). Whenever the DECtape control is writing, the circuit in the upper left corner of drawing RWBC generates a RWB(J) ⟶ WB pulse every TP0. This pulse, in turn, triggers either the WB ⟵ RWB(J)FWD or WB ⟵ RWB(J)REV pulse depending on the direction of tape motion.

The write buffer (WB) appears in drawing RWB at the upper right. Which of the two 3-bit bytes is currently to be written is determined by the state of TCT. Six NAND gates at 1A18 select the proper byte and present the resulting data to the write inputs of the Type 4523 Manchester Reader and Writer modules. The gates on these modules jam the 3-bit byte or its complement into the write buffer flip-flops as determined by the WB ⟵ RWB(J)FWD or WB ⟵ RWB (J) REV pulses.

One other signal required before write current is applied to the read-write heads; that signal is UT WREN DATA. This level which is asserted so long as data continues to be written, is interlocked with the WRITE LOCK switch on the selected transport. UT WREN DATA is developed on drawing UTC2. The UT WREN flip-flop at the top center of the drawing synchronizes UT WREN DATA with the necessary time pulses. This flip-flop is set to 1 on the first TP0 after the DECtape control becomes active and is not set back to 0 until TP4 after data transmission ceases. The WRITE LOCK switch of the selected transport is connected across pins B and J of plug 1B22. If the switch is open, writing is prevented and the UT WRITE PREVENT level is

generated. The 3-input NAND gate at the lower center of the drawing produces UT WREN DATA when UT WRITE, NOT UT WRITE PREVENT, and UT WREN(1) are all present. A copy of UT WREN DATA, UT WREN DATA (B), provides the additional power required to inhibit or enable all three write amplifiers.

At TP1, the write buffer flip-flops are complemented to record pulses of the desired polarity on the tape.

End of Data Transmission Operations

The above cycle of requesting a 6-bit byte, splitting the byte into two 3-bit bytes, and writing on the tape continues until the block mark end mark is read from the mark track. On TP1, the last bit comprising block-mark end shifts into the mark-track window. A NAND gate in the center of drawing RWBC develops the RW BM DONE level if the transmission of block-mark data is in progress when block-mark end is read. On the following TP2, a capacitor-diode gate in the upper right corner of drawing UTC2, enabled by RW BM DONE, sets the UT JB DONE FLAG to 1. On drawing RWBC, a capacitor-diode gate triggered by the transition of UT JB DONE FLAG places the triple-state flop into the null state to stop data transmission. Write current is not turned off until TP4 when the UT WREN flip-flop is reset to 0, ensuring that the last 3-bit byte has time to be written.

Write Data Operations

The write data operation is similar to the write block-mark operation; the same data flow path and most of the same control logic are used. Therefore, reference is made to the preceding paragraphs for a description of much of the data write logic.

Data Timing Register Operation

The data timing register (TDATA) is an 8-bit shift register appearing in drawing TMT. At TP2 time, this register is shifted one place if forward data end, reverse data end, or data sync appears in the mark-track window. A 1, shifted into TDATA0 when data sync is read, is shifted four times at the beginning and four times at the end of a data block. A brief study of the mark-track format shows that this 1 shifts into TDATA1 just before the reverse checksum slot,

is read, and shifts into TDATA6 just before the forward checksum slot. Thus, the more significant functions of the TDATA register occur when the 1 shifts into TDATA1 or TDATA6. Indeed, a NOR gate at the lower left of drawing RWBC develops the TDATA1 or 6 level.

Data Transmission Control

Data transmission control for writing data blocks is nearly the same as that for writing block marks. The tristable flop on drawing RWBC is placed in the RW RQ state in exactly the same way as for writing block marks. To enter the active state, the transition of TDATA1(1) triggers a capacitor-diode gate enabled by the AND of RW RQ and UT DATA (the read or write data command level).

Zero is written in the reverse checksum slot. During this slot, all data transmission operations occur as previously described except that production of the RWB ⟷ DC pulse (in the upper right of drawing RWBC) is inhibited by NOT TDATA1 or 6. Therefore, no data is requested from the data control and the read-write buffer remains cleared during the entire checksum slot. At the end of the checksum slot, the mark-track window decoder detects another reverse data-end mark, thereby shifting the 1 out of TDATA1 and into TDATA2. From the time until the forward checksum slot, data is requested from the data control and written on tape in exactly the same manner as for writing block-mark data.

Checksum Operations

One notable difference between writing block marks and writing data is the computation of the checksum in the longitudinal buffer (LB). The checksum is initialized to 0 by the LB CLEAR pulse, generated by a pulse amplifier at the top center of drawing RWBC on the transition of TDATA1(1) going to 1.

The timing for computing the checksum is not straightforward. On TP4 when TCT contains 0, the DECtape control requests and receives a new 6-bit byte from the data control. The following TP2, TCT complements from 0 (odd) to 1. The LB ⟵∨⟵ RWB pulse generated by a pulse amplifier at the top center of drawing RWBC is not produced on this TP2 because the capacitor-diode gate which triggers the pulse amplifier is not enabled for a sufficient length of time. Therefore, on the next TP2, the LB ⟵∨⟵ RWB pulse is produced, and, as shown on drawing

RWB, causes the exclusive OR of the LB and the RWB to replace the contents of the LB. One time pulse later, on TP3, the RWB contents are cleared in preparation for the next 6-bit byte.

When the checksum is about to be written at the end of the current data block, the 1 which is shifting through the TDATA register shifts into TDATA6. Once again the NOT TDATA1 or 6 level inhibits the request for another 6-bit byte from the data control. On the TP4 that would have requested a 6-byte, the RWB ⟵ LB(1) pulse is generated by the logic at coordinates A3 of drawing RWBC. Thus the first 6-bit byte to be written out in the checksum slot is the contents of the LB. As with any other 6-bit byte, the contents of the RWB are then exclusive ORed with the contents of the LB. Because any number exclusive ORed with itself yields zero, the LB becomes cleared. Therefore, the DECtape control fills out the checksum slot with zeros although the contents of the LB are transferred twice more to the RWB.

Skipping Over the Interblock Zone

If more than one data block is to be written at one time, the DECtape control must skip over the interblock zones so as not to disturb the reverse and forward block marks written there. If more data is ready in the data control, the NAND gate in drawing RWBC near coordinates B4 receives the following signals: DC SELECT 1 signifying that device 1 (the DECtape control) is slected by the data control; NOT DC DA RQ signifying that a 36-bit word is waiting in the data accumulator for transmission to the DECtape control; UT DATA signifying that the DECtape command is to write data blocks; and RW ACTIVE signifying that data transmission is in progress. The AND of these four signals is RW DATA CONT. In order to suspend data transmission for the duration of the interblock zone, the tristable flop is set to the RW RQ state by the output of a capacitor-diode gate enabled by RW DATA WR CONT and pulsed by the transition of TDATA6(0) going to 0 at the end of the checksum slot. Data transmission resumes in exactly the same way that transmission was begun initially; a data-sync mark-track code is read in the next data block, thus supplying another 1 to shift through the TDATA register.

End of Data Transmission Operations

Once the DECtape control begins to write a data block, it must write the entire block in order to have a valid checksum at both ends of the block. Writing ceases when the data control is no longer supplying data to the DECtape control. This condition is detected as shown on

drawing UTE by a NOR gate which generates the UTE DC DISCONNECT level whenever the data control does not select the DECtape control or when data is not ready for transmission to the DECtape control. The UTE DC DISCONNECT level, ANDed with RW ACTIVE and UT DATA on drawing RWBC becomes the RW DATA WR STOP level.

At the end of the next forward checksum slot, on the transition of TDATA6(0) going to 0, the output of a capacitor-diode gate in drawing UTC2 (upper right corner) sets the UT JB DONE FLAG flip-flop to 1 if RW DATA WR STOP is present. The UT JB DONE FLAG stops data transmission as described under the write block operation.

Write All Operation

The write all operation is identical to the write data operation except in the following two respects:

Reading the block-mark-sync mark-track code causes the DECtape control to enter the active state (see drawing RWBC). The RW RQ state is entered as described previously. Block-mark sync causes a 1 to shift into TBM0, also described previously. The transition of TBM0(1) going to 1 triggers a capacitor-diode gate to set the tristable flop to the RW ACTIVE state.

The DECtape control does not enter the RW RQ state during the interblock zones, but continues to write data. The checksum mechanisms function during the write all operation so that correct checksums are written automatically. Note that RW DATA WR CONT is the enabling level that allows the transition of TDATA6(0) going to 0 to place the tristable flop into the RW RQ state. This level cannot be present during read or write all operations because UT DATA (the read or write data command level) is one of the requirements for the generation of RW DATA WR CONT.

Read Operations

The differences between the read operations and the write operations are few. The principal difference is the reversal of the flow of data between the DECtape control and the data control. The logic that interprets the mark-track information is the same for both reading and writing. Only the differences are explained below.

Data Flow

Read amplifier strobe pulses are developed by the circuit in drawing RWBC at coordinates B2. At TP1 time, when in the active state and in the read mode, either the RWB ⟵ RAMP(1) CT(0) pulse or the RWB ⟵ RAMP(1) CT(1) pulse is generated depending on whether the first or the second three bits of each 6-bit byte are being read.

When reading in reverse, the complement obverse of the data is actually read from tape. The DECtape control recovers the true data by first taking the complement, then swapping bits to form the obverse. The direct data or the complement data is selected by NAND gates near the bottom of drawing RWB. The data is distributed through capacitor-diode gates to the inputs of the RWB by means of the RWB ⟵ RAMP(1) CT(0) and RWB ⟵ RAMP(1) CT(1) pulses. These gates only select the direct or the complement data; they do not swap bits to form the obverse.

When a 6-bit byte is assembled in the RWB, the data control is given one of the pulses, (LT) RWB ⟵ DC(1)FWD or (RT)RWB ⟵ DC(1)REV depending on the direction of tape motion. These pulses are triggered via the capacitor-diode gate input to the pulse amplifier in drawing RWBC at coordinates A7. It is instructive to review the timing sequence for the data flow during read operations. On a TP2 the DECtape control eventually becomes active with the count odd. On TP3, an RWB CLEAR pulse occurs, and on TP1 a read strobe pulse occurs. On the next TP2 the count becomes even and the capacitor-diode gate input to the pulse amplifier at 1B15 K and L (drawing RWBC, coordinates A7) becomes enabled (unless a checksum slot is being read). Since the trigger pulse (TP2) and the enabling level appear simultaneously, the gate does not produce an output pulse.

On the next TP1, the second three bits of data are strobed into the RWB. On TP2 the count goes from even to odd, but the capacitor-diode gate remains enabled long enough to trigger a RWB ⟷ DC pulse. The data control accepts the 6-bit byte and the cycle repeats.

The obverse of data read in reverse is formed at the data control. The 3-bit halves of each 6-bit byte are swapped at the input to the right end of the data accumulator, and the information is shifted to the right.

Checksum Operations

The formation of the checksum is controlled by exactly the same logic in reading and writing. A NAND gate in the lower right of drawing RWB detects when the LB contains 0. At the end of the checksum slot, when the 1 shifting through the TDATA register shifts into TDATA7, the LB contains the exclusive OR of all 6-bit bytes including both the reverse and forward checksums recorded on the tape. If the result is not zero, the UT INFO ERROR flip-flop in the upper right of drawing UTC2 is set to 1 to indicate an error.

Write Timing And Mark Track Operation

The write timing and mark track operation is the last discussion because this operation is so different from the others. During this operation, the timing and mark tracks written on the tape (if any) are ignored. Time pulses are provided by a clock shown in the lower right corner of drawing TMT. The UT WRTM level enables the clock to produce output pulses. The TCK register is a 2-bit counter which passes through the following states in the order specified:

Step	TCK1	TCK2	
1	0	0	
2	0	1	
3	1	1	
4	1	0	
1	0	0	(etc)

The TCK counter continually cycles through the above four states thereby dividing the clock rate by four. The transitions of the TCK1 flip-flop trigger the timing chain at the top of drawing TMT. These substitute time pulses are both written on the tape to generate the timing track and are used within the DECtape control to control the writing of the mark track.

Both the timing track and mark track write amplifiers are connected to the read-write heads through relay contacts. Thus, when the relay is not energized, it is impossible to erase the previous mark and timing track accidently. The relay is the UT BTM RELAY shown in the lower right corner of drawing UTC2. This relay, the UT BTM LIGHT, and the red lamps on each of the DECtape transports are controlled by the UT BTM WRITE SWITCH at 1A131. This switch also controls the UT BTM SW OFF level used in the error checking circuits to determine when an attempt is made to write the timing and mark tracks and the UT BTM WRITE SWITCH is off.

When the write timing and mark track operation is selected by a CONO command the following sequence of events takes place. The 551 enters the null state as described previously. A non-zero delay must be specified to enter the active state. Notice, in the lower right of drawing RWBC, that the capacitor-diode gate that normally sets up the RW RQ state is inhibited during the WRTM mode. Instead, the capacitor-diode gate at 1B7 pins H and J sets up the active state.

The normal shifting of the mark track window is inhibited by the capacitor-diode gate at the far left of drawing TMT. Thus, the usual block format control circuits are inoperative. The timing pulses read from the timing track are inhibited from driving the time-pulse chain by the NAND gate at the top center of drawing TMT.

The DECtape control requests 6-bit bytes from the data control in the same manner as during ordinary writing except that the TDATA register cannot inhibit the request for data (see the upper right corner of drawing RWBC). The data thus received is written on the tape in the same manner as in ordinary write operations. In addition, the data for channel 0 is applied to a NAND gate at the bottom left of drawing TMT, which passes the data on to the mark track write amplifier during WRTM operations. Thus, the mark track is a copy of the data written in channel 0.

One additional signal is present to enable the mark and timing track write amplifiers to write on the tape. This signal is the UT WREN BTM level derived at the bottom center of drawing UTC2 by the AND of UT WREN DATA (which prevents writing if WRITE LOCK is on), NOT UT BTM SW OFF (which is a double check to prevent writing if the UT BTM RELAY fails), and UT WRTM (the write timing and mark track command level).

Automatic Error Checking

Most error checking circuits appear on drawing UTE, although all error conditions result in setting flip-flops on drawing UTC2.

Mark Track Error Check

The mark track codes are checked as they appear in the mark track window to ensure that a valid code occurs exactly every six bit positions. The UTEK register is a 6-bit ring counter which contains a single 1 that cycles around. This register is shifted each TP2 unless the block mark space code appears.

When the initial command to the DECtape control is given with a nonzero delay, the TCLEAR pulse sets the UTECK flip-flop to 0. The output of this flip-flop, applied to the circuit in the lower left corner of drawing UTE, inhibits the UTE ERROR signal so that error detection does not begin immediately. The next important circuit action occurs when a 1 shifts into TBM3 at the start of a forward block mark. The 1 remains in TBM3 for two bit times. On the first bit time, the block mark space code is in the mark track window. Therefore, on TP3 the UTE PRESET 100000 pulse is generated to initialize the operation of the UTEK register. On the next TP3, the 1 is still in TBM3 but the block mark space code is shifted out of the mark track window. Therefore, on TP3, the UTECK flip-flop is set to 1, thereby enabling mark track error checking.

The UTEK register is shifted right one place by the UTE SH RT pulse on every TP2 except when the block mark space code appears in the mark track window. Since the block mark space code appears five times after the 1 shifts into TBM3, the shift right pulse is inhibited five times. Therefore, between the time that UTEK is preset to 100000 and the time the next-to-last bit of the block mark end code shifts into the mark track window, 11 bit times go by but only six shift pulses are generated. These six shifts cycle the 1 in the UTEK register back to UTEK1. The following TP1, the block mark end code appears in the mark track window. A NOR gate near the center of drawing UTE supplies the UTE MK level whenever any legitimate mark appears in the mark track window. Since the 1 in the UTEK register is in UTEK1 when the block mark end code appears, the UTE ERROR level is not asserted. If a mark track error had occurred, no legitimate mark would be present; therefore, the UTE ERROR level would be asserted since the 1 in UTEK1 signifies that a legitimate mark is expected. On TP2, a capacitor-diode gate enabled by UTE ERROR sets the UT INFO ERROR flip-flop (see drawing UTC2) if an error occurred.

After the initial steps described above, the UTEK register cycles around every six bit times. If a legitimate code occurs when not expected (UTEK1 containing 0) or no code occurs when expected (UTEK1 containing 1), the UTE ERROR level is asserted.

In order to avoid flagging an error when the reverse block mark code (45) or block mark space code appear, the UTEK flip-flop is reset to 0 on TP3 after block mark sync appears in the mark track window. The entire cycle described above repeats when a 1 again shifts into TBM3.

Active Error Check

If the DECtape control is active when the tape enters the interblock zone, an error has occurred. For example, if the DECtape control is writing data blocks, the active mode is in effect while writing is in progress. After writing the checksum, the DECtape control must enter the request state to avoid writing over the block marks written in the interblock zone. Similarly, if the DECtape control is active when the tape leaves the interblock zone and enters the data zone, an error has occurred. Both errors are detected by the circuit near the center of drawing UTE. Except in the read or write all modes in which it is desired to read or write through the interblock zone, the UTE ACTIVE ERROR level is asserted if the error condition arises. The presence of this level has two effects. First, on TP2 the UT INFO ERROR flip-flop on drawing UTC2 is set to 1 to indicate an error condition to the arithmetic processor. Second, the tristable flop on drawing RWBC is set to the RW NULL state, also on TP2, to terminate data transmission and prevent the possible loss of data.

Illegal Operation Error Check

The illegal operation error occurs when the DECtape control receives some command that cannot be accomplished due to the settings of the operator's control switches. For example, if a write operation is selected and the transport is in the WRITE LOCK mode, the UT WRITE PREVENT level is present. When the RWB (J)$\longrightarrow$ WB pulse occurs, indicating that a write operation is being attempted, the UT ILLEGAL OP flip-flop is set. As previously described, writing is inhibited by the UT WREN DATA level.

Two other error stiuations exist: two or more units (or zero units) are dialed to the selected transport number, or the UT BTM SWITCH position does not agree with the DECtape command. The analog circuit that detects when the wrong number of units are dialed to the selected unit number is described under Tape Unit Selection. Two NAND gates at the bottom of drawing UTE detect when the position of the UT BTM SWITCH disagrees with the DECtape command. The two error conditions are ORed to form the UTE SW ERROR level. This level is tested at the completion of the initial delay and sets the UT ILLEGAL OP flip-flop (see drawing UTC2) if an error is present.

Incomplete Block Detection

Although not necessarily an error, the reading or writing of an incomplete block sometimes indicates the loss of data and therefore is described in the same section as the other automatic error check circuits. The DECtape control leaves the active mode and sets the JOB DONE flag only at the end of a block of data or the end of a block mark word, depending on the command. If the data control disconnects at the end of a block of data, the DECtape control immediately enters the null state and requests no further data from the data control. If the data control disconnects at any other time, the DECtape control continues to request data until the end of the block. Thus, the RWB$\leftrightarrow$DC pulse occuring while the data control is disconnected indicates an incomplete block and sets the UT INCOMP BLOCK flip-flop as shown in drawing UTC2.

Status Checking Operations

The arithmetic processor may read back the contents of either the command register or the status register. The desired register is selected by sending the appropriate device number on the I/O bus as described under initialization operations. The IOB STATUS level is sent simultaneously to indicate that the DECtape control must place its status information on the bus. The UT STATUS and UTA STATUS levels, developed in the lower left of drawing UTC2, enable the necessary I/O bus drivers to place status information on the I/O bus.

Program Interrupt Operations

Any of five conditions in the DECtape control can be programmed to cause a program interrupt. Three of these conditions require that an enabling bit be set in the control register in order to affect the program interrupt. The circuit in the center of drawing UTC2 detects when any of the interrupt conditions is present. The two error flags, UT ILLEGAL OP and UT INFO ERROR, can cause an interrupt at any time. Three other flags; UT TIME FLAG, UT JB DONE FLAG, and UT TAPE END FLAG; can cause an interrupt only if the corresponding enable flip-flop contains 1. The OR of the five interrupt conditions is the UT INTERRUPT FLAGS level.

Three flip-flops in the control register; UT PIA33, UT PIA34, and UT PIA35 (see drawing UTC1); store the program interrupt channel number. The outputs of these flip-flops are applied to a

Binary-to-Octal Decoder Type 4151. Of the eight octal outputs, seven are applied to the seven interrupt lines of the I/O bus. The zero output is unused. The UT INTERRUPT FLAGS level is the enable input to the decoder. If the UT INTERRUPT FLAGS level is asserted, the interrupt line corresponding to the stored channel number is grounded thereby requesting an interrupt. Otherwise, all decoder outputs are inactive.

The arithmetic processor must remove the interrupt condition by sending the necessary CONO commands to the DECtape control.

CIRCUIT DISCUSSION

Three modules in the 551 deserve special attention either because of unusual complexity or because of unusual function. The three are the Manchester Reader and Writer Type 4523, the Mark Track Decoder Type 4260, and the Level Standardizer Type 1501. For an explanation of other module circuits, refer either to the System Modules Catalog C-100 or to Programmed Data Processor-6 Circuit Manual F-67 (166 Cir.).

Manchester Reader and Writer Type 4523

The Manchester Reader and Writer Type 4523 consists of separate amplifiers used to read and write one channel of a standard DECtape.

Read Amplifier

The read portion is a high gain differential amplifier and produces a usable -3 volt output signal with less than 1 millivolt of input signal from a grounded center-tap head. In use, the read amplifier input is connected to the tape recording head in parallel with the write amplifier output and full write voltage is delivered to the read amplifier input. Overload protection in the read amplifier permits reading of low level signals within 50 microseconds after writing. Operating frequency range is 16 to 35 kc.

Write Amplifier

The write amplifier consists of a write flip-flop, two high current drivers, and input logic circuitry. The high current drivers are connected to the ends of a grounded center-tap head.

The drivers are returned to -14 volts. Two watt resistors mounted on lugs on the module are used to limit the head current and may be changed in order to change this current. Head currents up to 150 milliamperes are permissible.

Inputs and Outputs

Complement Input - Standard DEC positive pulses applied to pin H at any rate up to 35 kc cause the write flip-flop to complement and the current through the head to reverse with each pulse.

In 1 - A ground level applied to pin K causes the flip-flop to assume a state that permits write current to flow into pin N when a strobe pulse is applied to pin J. A -3 volt level causes the write current to flow into pin M.

In 2 - A ground level applied to pin E causes the flip-flop to assume a state that permits write current to flow into pin M when a strobe pulse is applied to pin F. A -3 volt level causes the write current to flow into pin N.

Enable - A ground level on pin L disables both current drivers so that no write current flows. In order to begin writing on tape, pin L must be at -3 volts.

Strobe 1 - A standard positive pulse applied to pin J reads the data on pin K into the write flip-flop.

Strobe 2 - A standard positive pulse applied to pin F reads the data on pin E into the write flip-flop.

Writer Out - A maximum of 150 milliamperes and 14 volts are supplied from either pin M or N depending on the state of the write flip-flop and the enable input.

Reader In - Pins S and T are the inputs to the read amplifier. These pins are usually connected to pins M and N respectively and to the opposite ends of a center-tapped read-write head.

Reader Out - The reader outputs at pins Y and Z are standard DEC levels. The output at pin Y is the complement of the output at pin Z.

Adjustments

Two adjustments are provided on the read amplifier, one to set the operation point and the other to set amplifier balance. These adjustments are factory preset and should not be altered unless absolutely necessary.

Mark Track Decoder Type 4260

The mark track decoder is described here because of its unusual size and complexity. The 4260 contains a 9-flip-flop shift register, diode decoders, and nine output inverters. The decoders determine the presence of nine fixed marks as they pass through the shift register. Bit 9 is set but never cleared by a shift. Two pulse inverters are included, one for shifting, and one for clearing. This module is double length because of the large number of components it contains.

Inputs - The information input is at pin M. Ground at this input shifts a 1 into the register. The clear (pin H) and shift (pin J) pulse inputs accept standard negative 0.4 microsecond pulses.

Outputs - The outputs of both sides of flip-flops 8 and 9 appear on the module connector. For all four outputs, -3 volts represents assertion. These outputs are: flip-flop 8, 0 side, pin E; 1 side, pin P; flip-flop 9, 0 side, pin K; 1 side, pin L.

The nine decoder outputs are specified in the table below. The output at pin T is not used in the 551. For all outputs below, ground represents assertion.

Pin	Decoded Value	Mark Name
R	X25	block mark space
S	232	data sync
T	145	reverse block mark
U	222	forward end mark
V	351	block mark sync
Z	126	block mark end
Y	070	data
X	010 or 210	reverse data end
W	373 or 073	forward data end

The output of flip-flop 9 is included as part of all nine decoded values but is not explicitly included in the values given in the table.

Level Standardizer Type 1501

A description of the Level Standardizer Type 1501 appears in System Modules Catalog C-100 but is mentioned here because of the unusual application. This module consists of three differential amplifiers of which two are used in the 551. If pin J is more negative than pin H (or if pin M is more negative than pin N) the corresponding output inverter conducts. A 2-ohm resistor in series with the ground input to module 1C6 (the unit selection decoder) is effectively in series with the selection relays of any DECtape transport that is dialed to the selected unit number. The voltage developed across this resistor, the UT UNIT CHECK signal, is proportional to the number of units selected. If only one unit (the desired number) is selected, this voltage is in the range of .1 to .2 volts. Two potentiometers mounted behind connector 1B8 are adjusted to provide -0.1 and -0.2 volt references. The two differential amplifiers in the level standardizer detect that UT UNIT CHECK is within the desired range.

CHAPTER 4

INTERFACE

Logic interface signals sent and received by the DECtape control are standard DEC levels or pulses which are described in Appendix 1 of this manual. Tables 4-1 through 4-6 list the standard interface signals of the DECtape control and also list nonstandard interface signals such as the IOB POWER ON level (-15 volts). These tables, however, do not list the signals associated with interface connectors 1D13 through 1D16. Terminals on connectors 1D13, 1D14, 1D15, and 1D16 are parallel-connected to terminals identified by the same letter on interface connectors 1D12, 1D11, 1D10, and 1D9, respectively.

TABLE 4-1 INTERFACE SIGNALS FROM I/O BUS

Signal	Symbol	Connector/ Terminal	Destination	BS Drawing
IOB 1(1)	—◇	1D9-C	1D5Z	μTC1
IOB 2(1)	—◇	1D9-D	1C9L	μTC1
IOB 3(1)	—◇	1D9-E	1C9R	μTC1
IOB 4(1)	—◇	1D9-F	1C9V	μTC1
IOB 5(1)	—◇	1D9-H	1C9Z	μTC1
IOB 6(1)	—◇	1D9-K	1C3L	μTC1
IOB 7(1)	—◇	1D9-L	1C3R	μTC1
IOB 8(1)	—◇	1D9-M	1C3V	μTC1
IOB 9(1)	—◇	1D9-N	1C3Z	μTC1
IOB 10(1)	—◇	1D9-P	1C5L	μTC1
IOB 11(1)	—◇	1D9-R	1C5R	μTC1
IOB 12(1)	—◇	1D9-T	1C5V	μTC1
IOB 13(1)	—◇	1D9-U	1C5Z	μTC1
IOB 14(1)	—◇	1D9-V	1C7L	μTC1
IOB 15(1)	—◇	1D9-W	1C7R	μTC1

TABLE 4-1 INTERFACE SIGNALS FROM I/O BUS (continued)

Signal	Symbol	Connector/ Terminal	Destination	BS Drawing
IOB 16(1)	——◇	1D9-X	1C7V	μTC1
IOB 17(1)	——◇	1D9-Y	1C7Z	μTC1
IOB CONO CL	——▶	1D12-D	1C12K	μTC2
IOB CONO SET	——▶	1D12-E	1C12S	μTC2
IOB POWER ON (−15 v)		1D11-C	Power Control 811C	μTC2
IOB RESET	——▶	1D11-B	1C12E	μTC2
IOB STATUS	——◆	1D12-H	1C15R	μTC2
IOB STATUS	——◆	1D12-H	1C15U	μTC2
IOS 3(0)	——◇	1D11-F	1D17F	μTC2
IOS 4(1)	——◇	1D11-L	1D17H	μTC2
IOS 5(0)	——◇	1D11-M	1D17J	μTC2
IOS 6(0)	——◇	1D11-P	1D17K	μTC2
IOS 7(0)	——◇	1D11-T	1D17L	μTC2
IOS 8(1)	——◇	1D11-W	1D17M	μTC2
IOS 9(0)	——◇	1D11-X	1D17Y	μTC2
IOS 9(1)	——◇	1D11-Y	1D17N	μTC2

TABLE 4-2 INTERFACE SIGNALS TO I/O BUS

Signal	Symbol	Connector/ Terminal	Origin	BS Drawing
IOB 19(1)	——◇	1D10-C	1D7Z	μTC1
IOB 20(1)	——◇	1D10-D	1C11H	μTC1
IOB 21(1)	——◇	1D10-E	1C11E	μTC1
IOB 22(1)	——◇	1D10-F	1C11P	μTC1
IOB 23(1)	——◇	1D10-H	1C11T	μTC1
IOB 24(1)	——◇	1D10-K	1C2H	μTC1

TABLE 4-2 INTERFACE SIGNALS TO I/O BUS (continued)

Signal	Symbol	Connector/ Terminal	Origin	BS Drawing
IOB 25(1)	—◇	1D10-L	1C2L	μTC1
IOB 25(1)	—◇	1D10-L	1D8H	μTC2
IOB 26(1)	—◇	1D10-M	1C2P	μTC1
IOB 26(1)	—◇	1D10-M	1D8L	μTC2
IOB 27(1)	—◇	1D10-N	1C2L	μTC1
IOB 27(1)	—◇	1D10-N	1D8P	μTC2
IOB 28(1)	—◇	1D10-P	1C2W	μTC1
IOB 28(1)	—◇	1D10-P	1D8T	μTC2
IOB 29(1)	—◇	1D10-R	1C2Z	μTC1
IOB 29(1)	—◇	1D10-R	1D8W	μTC2
IOB 30(1)	—◇	1D10-T	1C10H	μTC1
IOB 30(1)	—◇	1D10-T	1D8Z	μTC2
IOB 31(1)	—◇	1D10-U	1C10L	μTC1
IOB 31(1)	—◇	1D10-U	1D7H	μTC2
IOB 32(1)	—◇	1D10-V	1C10P	μTC1
IOB 32(1)	—◇	1D10-V	1D7L	μTC2
IOB 33(1)	—◇	1D10-W	1C10T	μTC1
IOB 33(1)	—◇	1D10-W	1D7P	μTC2
IOB 34(1)	—◇	1D10-X	1C10W	μTC1
IOB 34(1)	—◇	1D10-X	1D7T	μTC2
IOB 35(1)	—◇	1D10-Y	1C10Z	μTC1
IOB 35(1)	—◇	1D10-Y	1D7Y	μTC2
P1 REQ1	—◇	1D12-R	1C8S	μTC1
P1 REQ2	—◇	1D12-T	1C8T	μTC1
P1 REQ3	—◇	1D12-U	1C8U	μTC1
P1 REQ4	—◇	1D12-V	1C8V	μTC1
P1 REQ5	—◇	1D12-W	1C8W	μTC1
P1 REQ6	—◇	1D12-X	1C8X	μTC1
P1 REQ7	—◇	1D12-Y	1C8Z	μTC1

TABLE 4-3 INTERFACE SIGNALS
FROM TYPE 555 TAPE TRANSPORTS

Signal Description	Symbol	Connector/ Terminal	Destination	BS Drawing
μT WRITE PREVENT enable	——◇	1B22-J	1B23K	μTC2
Ch 0 Read Data		1A22-Y	1A50V	RWB
Ch 0 Read Data		1A22-Z	1Z50J	RWB
Ch 1 Read Data		1A22-U	1A50T	RWB
Ch 1 Read Data		1A22-V	1A50L	RWB
Ch 2 Read Data		1A22-P	1A50R	RWB
Ch 2 Read Data		1A22-R	1A50N	RWB
Mark Track Read Data		1A22-F	1A55T	TMT
Mark Track Read Data		1A22H	1A55L	TMT
Timing Track Read Data		1A22-B	1A55R	TMT
Timing Track Read Data		1A22-C	1A55N	TMT

TABLE 4-4 INTERFACE SIGNALS
TO TYPE 555 TAPE TRANSPORTS

Signal Description	Symbol	Connector/ Terminal	Origin	BS Drawing
Select Tape Unit 1	——◇	1B22-X	1C6R	μTC1
Select Tape Unit 2	——◇	1B22-W	1C6S	μTC1
Select Tape Unit 3	——◇	1B22-V	1C6T	μTC1
Select Tape Unit 4	——◇	1B22-U	1C6U	μTC1
Select Tape Unit 5	——◇	1B22-T	1C6V	μTC1
Select Tape Unit 6	——◇	1B22-S	1C6W	μTC1
Select Tape Unit 7	——◇	1B22-R	1C6X	μTC1
Select Tape Unit 8	——◇	1B22-P	1C6P	μTC1
μT FWD	——◇	1B22-F	1B20L	μTC1
μT GO	——◇	1B22-E	1B21N	μTC1

TABLE 4-4 INTERFACE SIGNALS
TO TYPE 555 TAPE TRANSPORTS (continued)

Signal Description	Symbol	Connector/ Terminal	Origin	BS Drawing
Lamp 2 μT REVERSE	——◇	1B22-H	1B20N	μTC1
μT STOP	——◇	1B22-K	1B21L	μTC1
Ch 0 Write Data		1A22-Y	1A19N	RWB
Ch 0 Write Data		1A22-Z	1A19M	RWB
Ch 1 Write Data		1A22-U	1A20N	RWB
Ch 1 Write Data		1A22-V	1A20M	RWB
Ch 2 Write Data		1A22-P	1A21N	RWB
Ch 2 Write Data		1A22-R	1A21M	RWB
Mark Track Write Data		1A22-F	1A23N	TMT
Mark Track Write Data		1A22-H	1A23P	TMT
Timing Track Write Data		1A22-B	1A23R	TMT
Timing Track Write Data		1A22-C	1A23S	TMT

TABLE 4-5 INTERFACE SIGNALS FROM DATA CONTROL 136

Signal Description	Symbol	Connector/ Terminal	Destination	BS Drawing
Set gates (LT)RWB◀——DC(1) (LT) into RWB 0	——◆	1D25-K	1A12F	RWB
Set gates (LT)RWB◀——DC(1) (LT) into RWB 1	——◆	1D25-L	1A11F	RWB
Set gates (LT)RWB◀——DC(1) (LT) into RWB 2	——◆	1D25-M	1A10F	RWB
Set gates (LT)RWB◀——DC(1) (LT) into RWB 3	——◆	1D25-N	1A12T	RWB
Set gates (LT)RWB◀——DC(1) (LT) into RWB 4	——◆	1D25-P	1A11T	RWB
Set gates (LT)RWB◀——DC(1) (LT) into RWB 5	——◆	1D25-R	1A10T	RWB

TABLE 4-5 INTERFACE SIGNALS
FROM DATA CONTROL 136 (continued)

Signal Description	Symbol	Connector/ Terminal	Destination	BS Drawing
DC DARQ	——◆	1D25-W	1C19H	μTE
DC SEL 1	——◆	1D25-X	1D22E	RWBC
∿DC DARQ	——◇	1D25-W	1D23H	RWBC
∿DC SEL 1	——◇	1D25-X	1C20K	μTE
Set gates (RT)RWB◀——DC(1) (RT) into RWB 0	——◆	1D24-N	1A12J	RWB
Set gates (RT)RWB◀——DC(1) (RT) into RWB 1	——◆	1D24-P	1A11J	RWB
Set gates (RT)RWB◀——DC (1) (RT) into RWB 2	——◆	1D24-R	1A10J	RWB
Set gates (RT)RWB◀——DC(1) (RT) into RWB 3	——◆	1D24-K	1A12V	RWB
Set gates (RT)RWB◀——DC(1) (RT) into RWB 4	——◆	1D24-L	1A11V	RWB
Set gates (RT)RWB◀——DC(1) (RT) into RWB 5	——◆	1D24-M	1A10V	RWB

TABLE 4-6 INTERFACE SIGNALS TO DATA CONTROL 136

Signal	Symbol	Connector/ Terminal	Origin	BS Drawing
RWB 0(1)	——◆	1D25-B	1A16J	RWB
RWB 1(1)	——◆	1D25-C	1A16U	RWB
RWB 2(1)	——◆	1D25-D	1A15J	RWB
RWB 3(1)	——◆	1D25-E	1A16P	RWB
RWB 4(1)	——◆	1D25-F	1A16Z	RWB
RWB 5(1)	——◆	1D26-H	1A15P	RWB
(RT)RWB◀——▶DC(1)REV	——▶	1D25-T	1B15W	RWBC
(LT)RWB◀——▶DC(1)FWD	——▶	1D25-U	1B15P	RWBC

CHAPTER 5

PROGRAMMING

To be supplied

CHAPTER 6

MAINTENANCE

Maintenance of the DECtape control consists of procedures repeated periodically as preventive maintenance and tasks performed in the event of equipment malfunction as corrective maintenance. The procedures presented here assume that the reader is familiar with the operation of the DECtape control. Maintenance activities require use of the equipment listed in Table 6-1, or equivalent, as well as the use of standard hand tools, cleansers, and test cables and probes.

TABLE 6-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Model
Potentiometric dc Voltmeter	John Fluke	801H (0.025%)
Multimeter	Triplett or Simpson	630-NA or 260
Oscilloscope	Tektronix	540 Series
System Module Extender*	DEC	1954
System Module Puller*	DEC	1960
Small thin-bladed screw driver		
Phillips head screw driver		

*One supplied with the DECtape control

If it is necessary to remove modules during preventive or corrective maintenance, the Type 1960 System Module Puller should be used. Turn off all power before extracting or inserting modules. Carefully hook the small flange of the module puller over the center of the module rim, and gently pull the module from the mounting panel. Use a straight even pull to avoid damage to plug connections or twisting of the printed-wiring board. Since the puller does not fasten to the module, grasp the rim of the module to prevent it from falling. Access to controls on the module for use in adjustments or access to points used in signal tracing can be gained by removing the module, connecting a Type 1954 System Module Extender into the mounting panel, and then inserting the module into the extender.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of procedures performed prior to the initial operation of the DECtape control and periodically during its operating life to ensure that it is in satisfactory operating condition. Performance of these procedures will forestall possible future failure by correcting minor damage and discovering progressive deterioration at an early stage. A log book for recording data found during the performance of each preventive maintenance task will indicate the rate of circuit operation deterioration and provide information to determine when components should be replaced to prevent failure of the equipment. These tasks consist of mechanical checks which include cleaning and visual inspections; checks of specific circuit elements such as the power supply, clock timing, reader-writer adjustment and delay timing; and marginal checks, which aggravate borderline conditions or intermittent failures so that they can be detected and corrected. All preventive maintenance tasks should be performed every six months or 1000 equipment operating hours, whichever occurs first.

Mechanical Checks

Assure good mechanical operation of the DECtape control by performing the following steps and the indicated corrective action for any substandard conditions found:

1. Clean the exterior and the interior of the DECtape control using clean cloths moistened with nonflammable cleaning solvent or by means of a vacuum cleaner.

2. Clean the air filter at the bottom of the cabinet. Remove the filter by removing the fan and housing which are held in place by two knurled and slotted captive screws. Wash the filter in soapy water, dry in an oven or by spraying with compressed gas, and spray with Filter Kote (Research Products Corporation, Madison, Wisconsin).

3. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

4. Visually inspect the DECtape control for completeness and general condition. Repaint any scratched or corroded areas.

5. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.

6. Inspect the following for security: switches, controls, knobs, jacks, connectors, transformers, fan, capacitors, lamp assemblies, etc. Tighten or replace as required.

7. Inspect all racks of logic to assure that each module is securely seated in its connector.

8. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors exhibiting these signs of malfunction.

Type 728 Power Supply Check

Check the output voltage and ripple content of the 728 Power Supply and assure that it is within tolerance (see test data sheet for the particular supply). Use a multimeter to make the output voltage measurements without disconnecting the load. Use the oscilloscope to measure the peak-to-peak ripple content on the dc outputs of the supply. This supply is not adjustable, so if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be undertaken.

Check the +10-volt output between the black (-) and red (+) terminals to assure that it is between 9.5 and 11.0 volts with less than 800 millivolts ripple. Check the - 15-volt output to assure that it is between 14.5 and 16.0 volts with less than 400 millivolts ripple.

Type 1501 Level Standardizer Check

The procedure for checking and adjusting the 50-ohm potentiometers (1B38) associated with the Type 1501 Level Standardizer (1B8) is as follows:

1. Make certain that all registers in the DECtape control are clear. The registers are cleared each time the DECtape control is turned on.

2. Connect a jumper lead between ground and terminal 1C7H. This selects tape transport 1 by producing a ground level at 1C6R.

3. Turn the left transport selection switch located on tape transport 1 to position 1.

4. Turn the right transport selection switch to position 2.

NOTE: If correct indications cannot be obtained in steps 5, 6, or 7, the adjustment procedure given in step 7 should be performed.

5. Connect the oscillsocope to terminal 1C1V. The correct indication at this point is a -3-volt level.

6. Turn the right transport selection switch to position 1. The correct indication on the oscilloscope is a ground level.

7. Turn both transport selection switches to position 2. The correct indication on the oscilloscope is a ground level. If the correct indication cannot be obtained, the potentiometers (1B38) must be adjusted. As an approximate starting point, the upper potentiometer should be adjusted for a voltage reading of 0 volts measured from moveable arm to ground. The lower potentiometer should be adjusted for a voltage reading of approximately 0.27 volt measured from moveable arm to ground. If any adjustments are made during the performance of this procedure, the entire procedure should be repeated.

8. Remove the jumper lead connected between terminal 1C7H and ground.

Type 4303 Delay Check

The procedure for checking and adjusting the Type 4303 Delay (1D18) is as follows:

1. Connect a jumper lead between ground and terminal 1B118.

2. Connect the oscilloscope to terminal 1D18W. The correct indication at this point is a square-wave pulse which is at -3 volts for exactly 8 μsec and at ground for approximately 8 μsec. If this indication is incorrect, the adjustment screw (accessible through the hole in the handle of the Type 4303 module) must be turned.

3. Remove the jumper lead connected between terminal 1B118 and ground.

Type 4304 Delay Control Check

The procedure for checking and adjusting the Type 4304 Delay Control (1B3) is as follows:

1. Establish the following program to check the 35 msec delay:

```
        CONSZ UTS,   000020; skip if delay not through
Start   CONO UTC,    001000; set initial time of 35 msec
        JRST, .-2    jump back 2 instructions
```

2. Connect the oscilloscope to terminal 1B4W. The correct indication at this point is a negative level measuring approximately 3 volts in amplitude and 35 msec in duration. If this indication is not correct, the adjustment screw (accessible through the top hole in the handle of the Type 4304 module) must be turned.

3. Change the CONT UTC 001000 instruction to 010000. This selects an initial delay time of 225 msec.

4. Observe the oscilloscope. The correct indication is a negative level measuring approximately 3 volts in amplitude and ~~225~~ 180 – 199 msec in duration. If this indication is not correct, the adjustment screw (accessible through the second hole from the top of the Type 4304 module) must be turned.

5. Change the CONO UTC 001000 instruction to 011000. This selects an initial delay time of 300 msec.

6. Observe the oscilloscope. The correct indication is a negative level measuring approximately 3 volts in amplitude and 300 msec in duration. If this indication is not correct, the adjustment screw (accessible through the third hole from the top of the Type 4304 module) must be turned.

Type 4401 Variable Clock Check

The procedure for checking and adjusting the Type 4401 Variable Clock (1B18) is as follows:

1. Connect a jumper lead between ground and terminal 1B118.

2. Connect the oscilloscope to terminal 1B18F. The correct indication at this point is a positive pulse measuring 2.5 to 2.7 volts in amplitude and 8.33 μsec in duration. If this indication is incorrect, the adjustment screw (accessible through the hole in the handle of the Type 4401 module) must be turned.

3. Remove the jumper lead connected between terminal 1B118 and ground.

Type 4523 Manchester Reader/Writer Check

The following procedure for checking and adjusting any of the Type 4523 Manchester Read & Writer modules should only be performed by an experienced maintenance technician.

1. Remove jumpers at 1A50 and 1A55 and replace them with Type 1033 Attenuator modules.

2. Establish a test program which will rock the tape for periods of approximately 4 seconds.

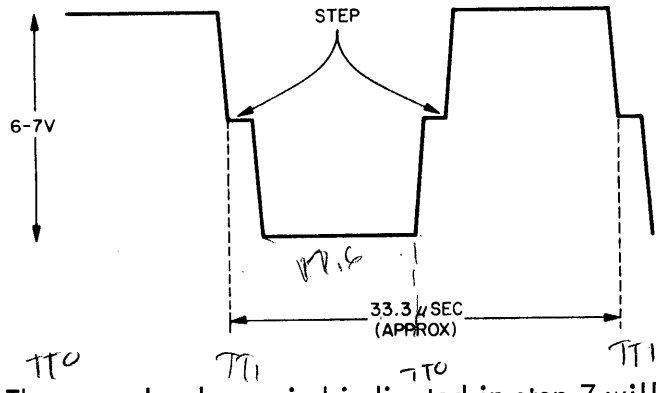
3. Use location 1A25 (timing track) to check any Type 4523 module. Remove the Type 4523 from location 1A25 (unless this module is being checked) and install the Type 4523 to be checked in location 1A25.

4. Turn the MODE switch of the oscilloscope to position ADDED ALGEBRAICALLY. Turn the POLARITY switch of channel A to position NORMAL (+). Turn the POLARITY switch of channel B to position INVERTED (-).

5. Connect the channel A input of the oscilloscope to terminal 1A25Y. Connect the channel B input to terminal 1A25Z.

NOTE: It may be necessary to replace one or both of the Type 1033 Attenuator modules with the jumpers in order to obtain the correct indication specified in step 6. However, vernier adjustments should be made with both Type 1033 modules installed.

6. Observe the oscilloscope. The correct indication is a square wave with an amplitude of 6 to 7 volts and a pulse period of approximately 33.3 μsec. If the correct indication is not obtained, turn the sensitivity potentiometer (accessible through the lower hole in the handle of the Type 4523 module) in one direction until a step appears in the square wave as shown below. Turn the potentiometer in the opposite direction until the step disappears and then reappears. Determine the adjustment range of the potentiometer by rocking it between the two limits which produce a step in the square wave. Permanently set the potentiometer to the center of this range.



NOTE: The normal pulse period indicated in step 7 will vary with the speed of the tape. Vernier measurements and adjustments should be performed with the tape advancing in the forward direction.

7. Observe the oscilloscope. The duty cycle of the square wave should be 50%. If the correct indication is not obtained, then the duty cycle potentiometer (accessible through the top hole in the handle of the Type 4523 module) must be adjusted. If an adjustment is made during this step, repeat steps 6 and 7 until the correct indication for these steps is observed.

8. Return any Type 4523 modules, removed during the performance of this test procedure, to their original locations.

9. Remove both Type 1033 modules and replace the jumpers at locations 1A50 and 1A55.

Read/Write Circuitry Check

The procedure for checking the various read/write circuits is performed with the use of two Type 1033 Attenuator modules as follows:

1. Remove jumper (1A50) and replace it with a Type 1033 module.

2. Remove jumper (1A55) and replace it with a Type 1033 module.

3. Run a program which utilizes all read/write circuits. If the program is run without interruption, the read/write circuits are functioning properly. The attenuated signals produced by the installation of the Type 1033 module will cause marginal read/write circuits to fail. The component which has failed can be detected by analyzing the point at which the program has stopped.

4. Remove both Type 1033 modules and replace the jumpers at locations 1A50 and 1A55.

Marginal Checks

Marginal checks are performed to aggravate borderline conditions within the logic circuits to reveal observable faults. Therefore these conditions can be corrected during scheduled preventive maintenance to forestall possible future equipment failure. These checks can also be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors. The checks are performed by operating the equipment logic circuits from an external, adjustable power source such as the DEC Type 734 Variable Power Supply. The marginal check panel of the PDP-6 has facilities for providing this power through a bus to the DECtape control. Raising the bias voltage above +10 volts is equivalent to lowering the amount of base drive on a particular transistor. This in turn simulates a lower gain driving transistor. Raising the bias voltage thus tends to indicate low gain transistors. Lowering the bias voltage below +10 volts simulates a condition where the voltage drop across the previous driving transistor (V_{ce}) has increased, thus tending to indicate high V_{ce} drop (leakage) transistors or low gain driving transistors. By raising or lowering the -15-volt supply margins, the delay and pulse amplifier modules may be checked. Raising or lowering the -15 volts does not affect the majority of control logic because -15 volts is the collector load voltage, which is usually clamped to -3 volts.

The +10-volt margin should be approximately ±8 volts and the -15 volt margin should be approximately ±3 volts. It is important that the -15-volt margin not be increased above -18 volts or damage can result within the logic circuits. By recording the level of bias voltage at which circuits fail, progressive deterioration can be plotted and expected failure dates predicted. Therefore these checks provide a means of planned replacement.

A color-coded connector at the right side of each rack of modules, as seen from the module side, provides connection to the normal and marginal operating voltage. Either the normal or marginal voltage supplied to the connector is selected for application to terminals A, B, and C of all modules in a rack by a switch at the end of the rack. Normal +10 and -15 volt lines are permanently connected to the output of the Type 728 Power Supply. Marginal +10 and -15 volt lines are common to all racks and are connected to the output of the Type 734 Variable Power Supply in the central processor via the I/O bus. The color coding of these connectors is as follows from top to bottom:

1. Green, +10 vdc internal marginal-check supply
2. Red, +10 vdc normal internal supply
3. Black, ground
4. Blue, -15 vdc normal internal supply
5. Yellow, -15 vdc external marginal-check supply

Three, single-pole, double-throw switches at the end of each rack of logic allow selection of either the normal or the marginal-check power supply (for distribution to the logic). The top switch connects the +10-volt supply to terminal A of all modules in that rack. In the down position, the fixed internal +10-volt supply (connected to the red terminal of the Type 728) is supplied to the modules; and in the up position, the marginal-check voltage (supplied to the green terminal from the power bus) is applied to terminal A of the modules. The center switch performs the same selection as the top switch for application of a nominal +10-volt level to terminal B of all modules. The bottom switch selects the -15-volt supply to be routed to terminal C of all modules. In the down position, the fixed -15-volt output of the 728 Power

Supply (blue terminal) is supplied to the modules; in the up position, the externally supplied marginal-check voltage (yellow terminal) is applied to terminal C of the delay and pulse amplifier modules only.

CAUTION

Make certain that all marginal check on/off switches on each rack of logic are off before performing the following procedure. Otherwise, damage to individual logic modules may result.

To perform the checks:

1. Energize the marginal check supply and adjust the outputs to supply the nominal +10 and -15 volt outputs.

2. Start equipment operation in a repetitive program or in a routine which fully utilizes the circuits in the rack to be tested.

3. Set the top switch on the rack to be checked to the up position.

4. Lower the +10-volt marginal-check power supply until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired.

5. Start equipment operation. Then increase the +10-volt marginal-check supply until normal operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced.

6. Reset the top switch to the down position.

7. Repeat steps 2-6 using the center switch on the logic rack being checked.

8. Repeat steps 2-6 using the bottom switch on the logic rack being checked while adjusting the -15-vdc marginal-check supply.

9. Reset the marginal-check power supply switch to the OFF position.

Timing Checks

Periodic checks of timing pulses should be made in accordance with the block schematics and timing charts for the DECtape control.

CORRECTIVE MAINTENANCE

The DECtape control is constructed of highly reliable transistorized modules. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment downtime due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. No special tools nor test equipment is required for corrective maintenance other than a broad bandwidth oscilloscope and a standard multimeter. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the operation of specific circuits, program techniques, the engineering drawings, and the location of mechanical and electrical components as described in this manual.

Diagnosis and remedial action for a fault condition are performed in the following phases:

1. Preliminary investigation to gather all information and to determine the physical and electrical security of the system.

2. System troubleshooting to locate the fault to within a module through the use of control panel troubleshooting, signal tracing, or aggravation techniques.

3. Circuit troubleshooting to locate defective components within a module.

4. Repairs or replacement to correct the cause of the malfunction.

5. Validation tests to assure that the malfunction has been corrected.

6. Log entry to record pertinent data.

Preliminary Investigation

It is virtually impossible to outline any specific procedures for locating faults within digital systems such as the DECtape control. Before commencing troubleshooting procedures, explore every possible source of information. Ascertain all possible information concerning any unusual function of the equipment prior to the fault and all possible program information such as routine in progress, condition of maintenance indicators, etc. Search the maintenance log to determine if this type of fault has occurred before or if there is any cyclic history of this kind of fault, and determine how this condition was previously corrected. When the entire machine fails, perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Assure that the power supplies are functioning properly and that there are no power short circuits by performing the power supply checks as described under Preventive Maintenance.

System Troubleshooting

Do not attempt to troubleshoot the DECtape control without first gathering all information possible concerning the fault, as outlined in the Preliminary Investigation.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. Careful checks should be made to assure that the DECtape control is actually at fault before continuing with corrective maintenance procedures. Faults in equipment transmitting or receiving information or improper connections within the system frequently produce indications very similar to those caused by a DECtape malfunction. From that portion of the program being performed and the general condition of the maintenance indicators, the logical section of the machine at fault can usually be determined.

DECtape Control Troubleshooting

If the fault has been traced to the DECtape control but cannot be localized to a specific logic function, perform the Microtog 6 diagnostic program procedure. When the location of a fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. Use the oscilloscope to trace signal flow through

the suspect logic element. Oscilloscope sweep may be synchronized by control signals or clock pulses available at individual module terminals. Trace the signal from the output back to its origin. The signal tracing method determines with absolute certainty the quality of pulse amplitude, duration, rise time, and the correct timing sequence In the event thatan intermittent malfunction exists, signal tracing must be combined with an appropriate form of aggravation test.

Aggravation Test

Intermittent faults should be traced through aggravation techniques. Intermittent failures caused by poor wiring connections can often be detected by vibrating the modules while the DECtape control is in operation. Often, wiping the handle of a screw driver across the back of a suspect row of modules is a useful technique. By repeatedly starting the DECtape control and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the module connection pins for signs of wear or misalignment, and check the module wiring for cold solder joints or wiring kinks.

Spare Parts Program

Any corrective maintenance program established for the DECtape control can be further implemented by an effective spare parts program. The program outlined in the following paragraphs lists recommended spare parts (modules, semiconductors, pulse transformers, and other miscellaneous components) to be stocked at the installation site of the DECtape control. The exact quantity of each spare part to be maintained can be varied to conform with the operating schedule and requirements of each individual user.

Module Spares

The following is a list of modules produced by DEC which are recommended as spares. One module of each type listed should be kept in stock.

4111	4217
4112	4221
4113	4260
4114	4151
4115	4671

6113	4303
6118	4304
6119	4127
4657	4129
4102	4604
6102	4606
6105	4681
6106	4410
4202	4401
4215	1501
4216	4523
	1802

Semiconductor Spares

A list of recommended semiconductor spares is presented in Table 6-2.

TABLE 6-2 SEMICONDUCTOR SPARES

Type	Vendor	Recommended Quantity
1N270	Transistron	1
1N276	Transistron	40
1N645	Transistron	25
1N994	Transistron	4
1N1217	GE	2
1N1220	GE	1
1N429 (Zener)	Motorola	1
1N3316 (Zener)	Motorola	1
GRS20SP4B4	GE	1
2N456A	RCA	2
2N485	Sprague	2
2N489	Sprague	5
2N599	GE	10
2N711A	GE	5
2N1184	RCA	5
2N1184B	RCA	2
2N1204	Motorola	4
2N1304	GE	2
2N1305	GE	10
2N527	GE	5
2N2451	Sprague	15
*2N1754	Gen. Inst.	5
2N1754	Gen. Inst.	10
2N393	Gen. Inst.	2

*BVCES 40V at 100 μa

Pulse Transformer Spares

A list of recommended DEC pulse transformer spares is presented in Table 6-3.

TABLE 6-3 PULSE TRANSFORMER SPARES

Type	Recommended Quantity
T2003	3
T2006	1
T2010	2
T2012	1
T2017	1
T2018	2
T2019	1
T2020	1
T2021	1
T2023	1
T2024	2
T2029	2
T2033	1

Miscellaneous Spares

A list of recommended miscellaneous component spares is presented in Table 6-4.

TABLE 6-4 MISCELLANEOUS SPARES

Component	Vendor	Part No.	Quantity
Indicator Light	Transistor Electric	MCHS-639B	6
Toggle Switch	Micro Switch	6AT4 (DPDT)	1
Rotron Fan	Micro Switch	53E168, Type CFG	1
Rotron Filter	Micro Switch	130-34-X1431	4
Muffin Fan	DEC		1
Muffin Filter	DEC		1

Circuit Troubleshooting

Troubleshooting procedures for defective circuits within the DECtape control can be performed as on-line dynamic tests or can be performed at a bench as either static or dynamic tests. Circuit schematics of each module are supplied in Appendix 1 of this manual and should be referred to for detailed circuit information.

On-Line Dynamic Tests

Where downtime is not critical, the spare parts list can be reduced and signal tracing techniques can be utilized for troubleshooting modules within the DECtape control. This practice involves module removal using a Type 1906 System Module Puller, insertion of a Type 1954 System Module Extender into the module mounting panel, and insertion of the suspect module in the module extender. Oscilloscope signal tracing of the module, with the equipment operating in a program which exercises the module, may now be performed.

Static Bench Tests

Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter. When checking semiconductor devices, the X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistance of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same and no parallel paths exist, replace the diodes.

Measure the emitter-collector and emitter-base resistances of transistors. Most catastrophic failures are caused by short circuits between the collector and the emitter or are caused by an

open circuit in the base-emitter path. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exists between the emitter and base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions, a transistor can be considered as two diodes connected back-to-back. In this analogy, PNP transistors are considered to have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors, the base is assumed to be a common-anode connection, and both the emitter and collector assume the function of a cathode.

Multimeter polarity must be checked before measuring resistances since many meters (including the Triplett 630) apply a positive voltage to the common lead in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings provide no guarantee that the transistor is functioning properly. A more reliable indication of diode or transistor malfunction is obtained by using one of the many inexpensive in-circuit testers commercially available.

Damaged or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range, and connect it across the suspected connection. Probe the wires or components around the connection, or rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short durations, caused by an intermittent connection, can be detected by connecting a 1.5-volt flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope while probing the connection.

Dynamic Bench Tests

Dynamic bench testing of modules can be performed through the use of special equipment. A Type 922 Test Power Cable and either a Type 722 or Type 765 Power Supply can be used to energize a system module. These supplies provide both the +10-vdc and -15-vdc operating levels for the module in addition to ground and -3-volt levels which may be used to simulate signal inputs. The signal input potentials can be connected to any terminal normally wired to

receive logic level signals by eyelets provided on the power cable. Type 911 Patch Cords are used to make these connections between eyelets on the plug. In this manner, logic operations and voltage measurements can be made throughout the circuit. When using the Type 765 Bench Power Supply, marginal checks of an individual module can also be performed.

Repair

In all soldering and unsoldering operations performed in the repair or replacement of components, avoid placement of excessive solder or flux on adjacent components or service lines. When soldering semiconductor devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the following special precautions should be taken:

1. Use a heat sink, such as a pair of needle-nose pliers, to grip the lead between the device and the connection being soldered.

2. Use a 6-volt soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

3. Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module etched wiring.

When any component of the equipment is removed for repair or replacement, make certain that all leads or wires which are unsoldered or otherwise disconnected are legibly tagged or marked for identification with their respective terminals. Replace defective components with those of equal or greater quality and equal or narrower tolerance.

Validation Test

Following the replacement of any electrical component of the DECtape control, a test should be performed to assure the correction of the fault condition and to make any readjustments of timing or signal levels affected by the replacement. This test should be taken from the preventive maintenance procedure most applicable to the portion of the system in which the error was found. For example, if a filter capacitor was replaced in one of the power supplies, the ripple check for that power supply should be repeated as specified under Power Supply Checks. Or, if the Type 4401 Variable Clock is replaced, the associated test procedure for this module

should be performed. If repair or replacement is performed in any area which is not checked during preventive maintenance, an appropriate operational test should be devised. For example, if a flip-flop is replaced, the control function performed by the flip-flop should be completely checked by manual setting and clearing or by programmed exercise of the function.

Log Entry

Corrective maintenance activities are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments which would be helpful in future maintenance.

APPENDIX 1

ENGINEERING DRAWINGS

This appendix contains reduced copies of the block schematics, circuit schematics, and other engineering drawings necessary for understanding and maintaining this equipment. Only those drawings which are essential and are not available in the referenced pertinent documents are included. Refer to the table of contents for a list of these drawings.

A complete set of engineering drawings is supplied with the equipment. Should any discrepancy exist between the drawings in this appendix and those supplied, assume that the latter drawings are correct.

DRAWING NUMBERS

Engineering drawing numbers contain five items of information, separated by hyphens. This information consists of a 2-letter code specifying the type of drawing, a 1-letter code specifying the size of the drawing, the type number of the equipment, the manufacturing series of the equipment, and a code specifying the drawing within a particular series. The drawing type codes are:

BS, block schematic or logic diagram
CD, cable diagram
CS, circuit schematic
FD, flow diagram
ID, interconnection drawing
PW, power wiring
RS, replacement schematic
SD, system diagram
TD, timing diagram
TFD, timing and flow diagram
UML, utilization module list
WD, wiring diagram

CIRCUIT SYMBOLS

The block schematics of Digital equipment are multipurpose drawings that combine signal flow, logical function, circuit type and location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using special symbols that define the circuit operation. These symbols are similar to those in the Digital System Modules Catalog but are often simplified. Figure A1-1 illustrates some of the symbols used in Digital engineering drawings.

LOGIC SIGNAL SYMBOLS

A digital logic signal symbol is shown at the input of almost all circuit symbols to specify the assertive conditions required to produce a desired output.

All logic signals are either standard Digital logic levels or standard Digital pulses. The standard Digital logic level is either at ground (0 to −0.3 v) or at −3 v (−2.5 to −3.5 v). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (——◇) indicates that the signal is a level and that ground represents assertion; a solid diamond (——◆) indicates that the signal is a level and that −3 v represents assertion. All logic levels applied to the conditioning-level inputs of capacitor-diode gates must be present for either 1 or 3 μsec (depending on the module used) before an input triggering pulse is applied to the gate.

The standard Digital negative pulse is indicated by a solid triangle (——▶) and goes from ground to −3 v (−2.5 to −3.5-v tolerances). The standard Digital positive pulse, indicated by an open triangle (——▷), goes either from −3 v to ground or from ground to +2.5 v (+2.3 to +3.0 v). The width of the standard pulses used in this equipment is either 1.0, 0.4, or 0.07 μsec, depending on the module and application.

Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (——◆▷) is drawn to indicate this fact. The triangle is drawn open or solid depending respectively on whether the positive (−3 v to ground) or the negative (ground to −3 v) transition triggers circuit action. The shading of the diamond either is the same as that of the triangle to indicate triggering on the leading edge of a level, or is opposite that of the triangle to indicate triggering on the trailing edge. Nonstandard signals are indicated by an arrowhead (——➤) pointing in the direction of signal flow.

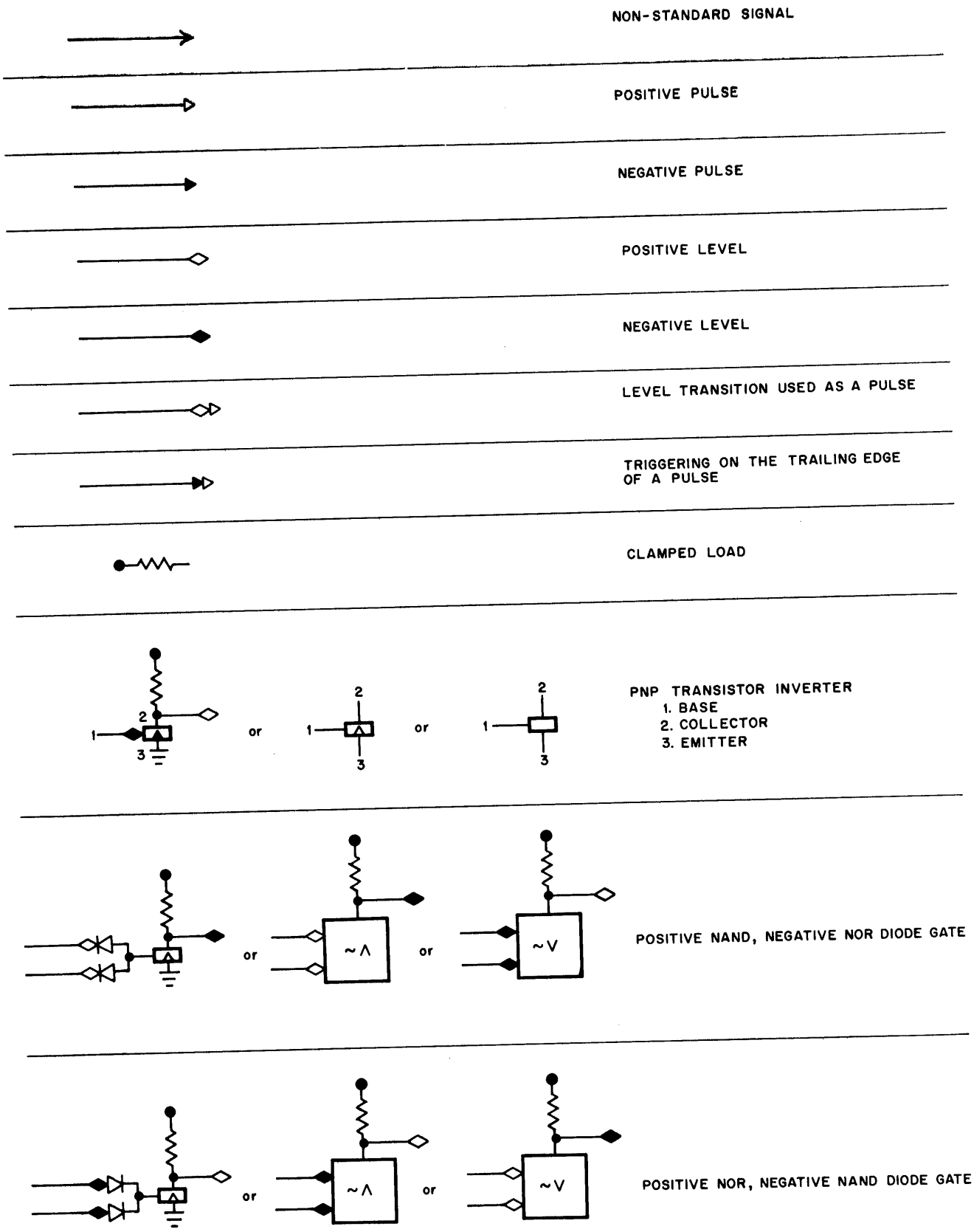
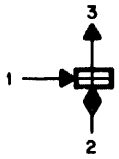


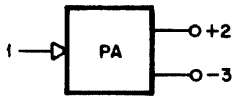
Figure A1-1 Circuit Symbols



CAPACITOR-DIODE GATE, POSITIVE OR NEGATIVE INDICATED BY POLARITY OF THE INPUTS.

1. PULSE INPUT
2. CONDITIONING LEVEL INPUT
3. PULSE OUTPUT

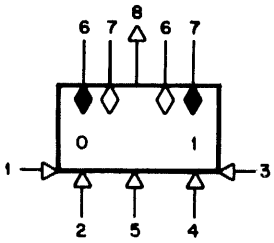
PULSE INVERTER



PULSE AMPLIFIER

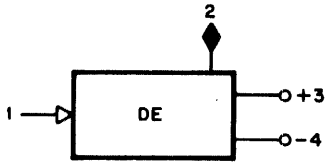
1. PULSE INPUT, POLARITY INDICATED BY INPUT SIGNAL

2,3. TRANSFORMER-COUPLED PULSE OUTPUT



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING):

1. DIRECT-CLEAR INPUT
2. GATED-CLEAR INPUT
3. DIRECT-SET INPUT
4. GATED-SET INPUT
5. COMPLEMENT INPUT
6. OUTPUT LEVEL, -3 V IF 0, 0 V IF 1
7. OUTPUT LEVEL, 0 V IF 0, -3 V IF 1
8. CARRY PULSE OUTPUT



DELAY (ONE-SHOT MULTIVIBRATOR)

1. INPUT PULSE
2. OUTPUT LEVEL, -3V DURING DELAY

3,4. TRANSFORMER-COUPLED PULSE OUTPUT

Figure A1-1 Circuit Symbols (continued)

COORDINATE SYSTEM

Each engineering logic drawing is divided into 32 zones (4 horizontal, and 8 vertical) by marginal map coordinates. Figure references in the text are usually followed by a letter and a digit specifying the zone in which the referenced circuit is located. Physical reference to a drawing area such as "lower left" or "upper center" may also be used.

MODULE IDENTIFICATION

Modules comprising the DECtape control are mounted on four mounting panels. The panels are identified by the letters A, B, C, and D, with A at the top. As viewed from the wiring side of the mounting panels, module locations (including blank locations) are numbered 1 through 25 from left to right. Individual terminals on each module connector are designated from top to bottom by the letters A through Z. The letters G, I, O, and Q are omitted from the lettering sequence.

Two designations appear in or near each circuit symbol or inside the dotted line surrounding multiple circuit symbols shown on engineering drawings. The upper designation is usually a 4-digit number specifying the module type. Standard modules are identified by this number in the Digital System Modules Catalog. Modules not described in the catalog are described in this manual or in the referenced pertinent documents.

The lower designation is the module location code. The leftmost character of this designation is a number indicating the cabinet or rack in which the module is located. Since all modules comprising the DECtape control are located in one rack, this number will always be a 1. The next character is a letter indicating the mounting panel in which the module is located. The last character consists of one or two numbers specifying the module location within the mounting panel. As an example, the designation 1A22 indicates that this module is mounted in location 22 of mounting panel A in rack 1. Terminal C of this module is designated as 1A22C.

Module connector terminals are identified by letters next to the circuit symbol. To identify a particular terminal, the terminal letter is added to the module location as a suffix. See Figure A1-2 for examples.

EXAMPLE

Figure A1-2 illustrates Digital symbols and nomenclature. The circuit shown is a Type 4303 Integrating Single Shot used to control the enabling time of several gates. The module is located in the twelfth position from the left (when viewed from the front or wiring side) of mounting panel B (the second from the top) in cabinet 1. The symbol marked DELAY is a monostable multivibrator with two complementary outputs, terminals U and W. In the 0 state, these terminals are at −3 v and ground as shown by the diamonds inside the symbol on the left. The −3 v from terminal U is the assertive level for a gate in 2D18 and is applied to terminal F as the SAFE signal. When the multivibrator is triggered, it momentarily goes to the 1 state and terminals U and W reverse their voltage levels, as shown by the diamonds representing the 1 state conditions. Terminal U now provides a ground assertive level to terminal M of a gate in 1B15, and terminal W provides a −3 v assertive level to terminal F of a gate in 1D02. The time the multivibrator remains in the 1 state is a function of the capacitor selected by jumpering terminal D to terminal E and the setting of the external potentiometer between terminals X and Z.

The multivibrator is triggered to the 1 state when any one of three signals occurs. One of these is a positive pulse designated GO from a pulse amplifier in 1C12. Another is a negative pulse designated SAMPLE from a NOR gate in 1C21, which is applied to the base of an inverter. The third is the positive transition at the trailing edge of the START signal, a negative level from a delay in 1B11. This will only trigger the capacitor-diode gate when a ground signal designated OPEN from a flip-flop in 1B13 has been present for at least 1 μsec.

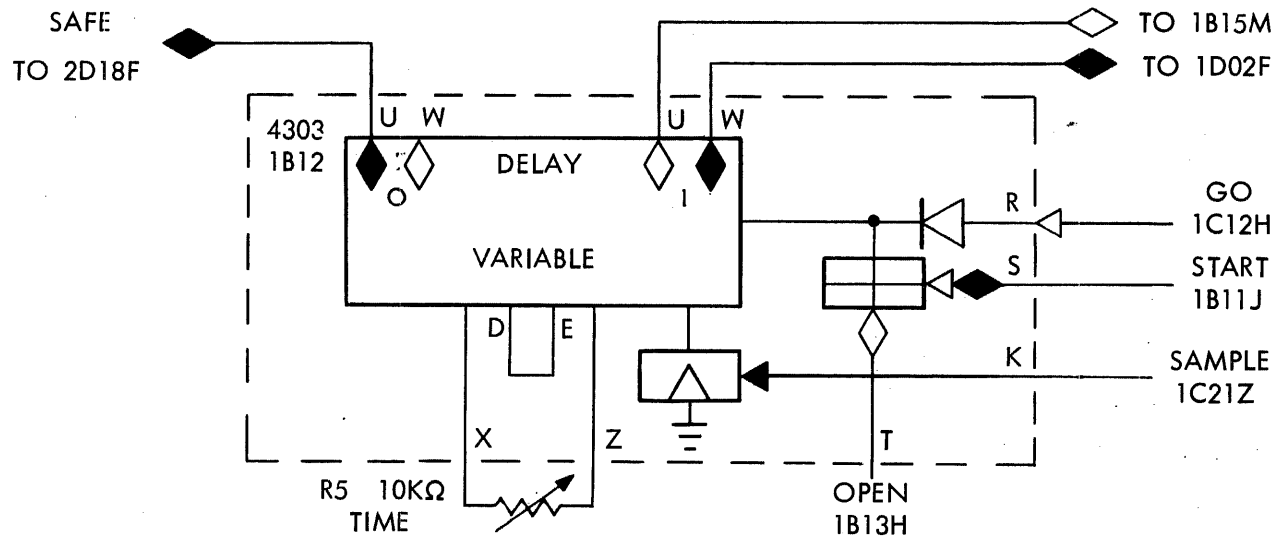


Figure A1-2 Typical Digital Logic Block Diagram